$1.75

EXAR

PHASE-LOCKED LOOP DATA BOOK

First in Quality...First in Service • Custom, Semicustom and Standard IC's

INTRODUCTION

This Data Book contains a complete summary of technical data and information covering Exar's complete line of Phase-Locked Loop (PLL) IC products. Each of the products presented in this Data Book covers a wide range of applications which will greatly simplify most system designs. To help the designer to find the right devices for his applications, a number of convenient cross-reference charts are also included which show the key features of each of the products discussed, in terms of different classes of applications.

EXPERIENCE AND PRODUCTS

Exar's innovativeness, product quality and responsiveness to customer needs have been the key to its success. Exar today offers a broad line of linear and interface circuits. In the field of standard linear IC products, Exar has extended its circuit technological leadership into the areas of communications and control circuits. Today Exar has one of the most complete lines of IC oscillators, timing circuits and phase-locked loops in the industry. Exar also manufactures a large family of telecommunication circuits such as tone decoders, compandors, modulators, PCM repeaters and FSK Modem Circuits. In the field of industrial control circuits, Exar manufactures a broad line of quad and dual operational amplifiers, voltage regulators, radio-control and servo driver IC's, and power control circuits.

Exar's experience and expertise in the area of bipolar IC technology extends both into custom and standard IC products. In the area of custom IC's, Exar has designed, developed, and manufactured a wide range of full-custom monolithic circuits, particularly for applications in the areas of telecommunications, consumer electronics, and industrial controls.

In addition to the full-custom capability, Exar also offers a unique semicustom IC development capability for low to medium-volume custom circuits. This semi-custom program, is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turn-around time of several weeks at a small fraction of the cost of a full-custom development program.

Exar's products are available in a variety of standard packages, or in die form for hybrid assemblies.

EXCELLENCE IN ENGINEERING

Exar quality starts in Engineering where highly qualified people are backed up with the advanced instruments and facilities needed for design and manufacture of custom, semi-custom and standard integrated circuits. Exar's engineering and facilities are geared to handle all three classes of IC design: (1) semi-custom design programs using Exar's bipolar and I^2L master chips; (2) full- custom IC design; (3) development and high-volume production of standard products.

Some of the challenging and complex development programs successfully completed by Exar include analog compandors and PCM repeaters for telecommunication, electronic fuel-injection, anti-skid braking systems and voltage regulators for automotive electronics, digital voltmeter circuits, 40-MHz frequency synthesizers, high-current and high-voltage display and relay driver IC's and many others.

NEW TECHNOLOGIES

Through company sponsored research and development activities, Exar constantly stays abreast of all technology areas related to changing customer needs and requirements. Exar has recently completed development efforts in Integrated Injection Logic (I^2L) technology, which offers unique advantages in the area of low-power, high-density logic arrays. Exar has a complete design engineering group dedicated to this new technology, and is currently supplying over twenty different custom and semi-custom I^2L products.

Using advanced processing technologies such as ion-implantation and multi-layer metal interconnections, Exar has developed a number of unique precision linear and digital LSI circuits for military and commercial applications.

FIRST IN QUALITY

From incoming inspection of all materials to the final test of the finished goods, Exar performs sample testing of each lot to ensure that every product meets Exar's high quality standards. Exar's manufacturing process is inspected or tested in accordance with its own stringent Quality Assurance Program, which is in compliance with MIL-Q9858A. Additional special screening and testing can be negotiated to meet individual customer requirements.

Throughout the wafer fab and assembly process, the latest scientific instruments, such as scanning electron microscopes, are used for inspection, and modern automated equipment is used for wafer probe, AC, DC, and functional testing. Environmental and burn-in testing of finished products is also done in-house. For special environmental or high reliability burn-in tests outside testing laboratories are used to complement Exar's own extensive in-house facilities.

FIRST IN SERVICE

Exar has the ability and flexibility to serve the customer in a variety of ways from wafer fabrication to full parametric selection of assembled units for individual customer requirements. Special marking, special packaging and military screening are only a few of the service options available from Exar. We are certain that Exar's service is flexible enough to satisfy 99% of your needs. The company has a large staff of Applications Engineers to assist the customer in the use of the product and to handle any request, large or small.

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Fundamentals of Phase-Locked Loops

The phase locked loop provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 1, the PLL in its most basic form is a feedback system comprised of three basic functional blocks: a phase comparator, low-pass filter and voltage controlled oscillator (VCO).

The basic principle of operation of a PLL can briefly be explained as follows: With no input signal applied to the system, the error voltage V_d is equal to zero. The VCO operates at a set frequency, f_o, which is known as the free-running frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to synchronize, or lock, with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a PLL system are its lock and capture ranges. They can be defined as follows:

Lock range: The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the tracking or holding range. Lock range increases as the over-all gain of the PLL is increased.

Capture range: The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It decreases as the filter bandwidth is reduced.

The lock and the capture ranges of a PLL can be illustrated with reference to Figure 2, which shows the typical frequency-to-voltage characteristics of a PLL. In the figure, the input is assumed to be swept slowly over a broad frequency range. The vertical scale corresponds to the loop error voltage.

In the upper part of Figure 2, the loop frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency f_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input, causing a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of the VCO voltage-to-frequency conversion gain, and goes through zero as $f_s = f_o$. The loop tracks the input until the input frequency reaches f_2, corresponding to the upper edge of the lock range. The PLL then loses lock, and the error voltage drops to zero.

If the input frequency is now swept slowly back, the cycle repeats itself as shown in the lower part of Figure 2. The loop recaptures the signal at f_3 and traces it down to f_4. The frequency spread between (f_1, f_3) and (f_2, f_4) corresponds to the total capture and lock ranges of the system; that is, $f_3 - f_1$ = capture range and $f_2 - f_4$ = lock range. The PLL responds only to those input signals sufficiently close to the VCO frequency, f_o, to fall within the "lock" or "capture" range of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_o.

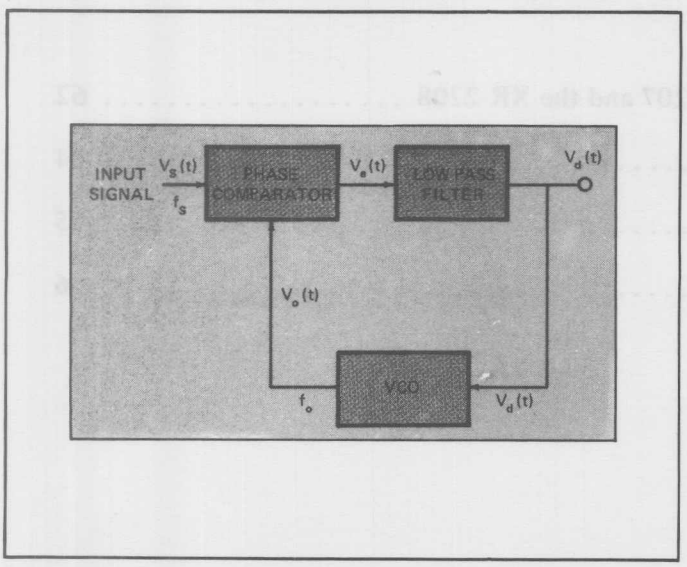


Figure 1. The basic phase locked loop consists of three functional blocks: a phase comparator, a low pass filter and a voltage-controlled oscillator.

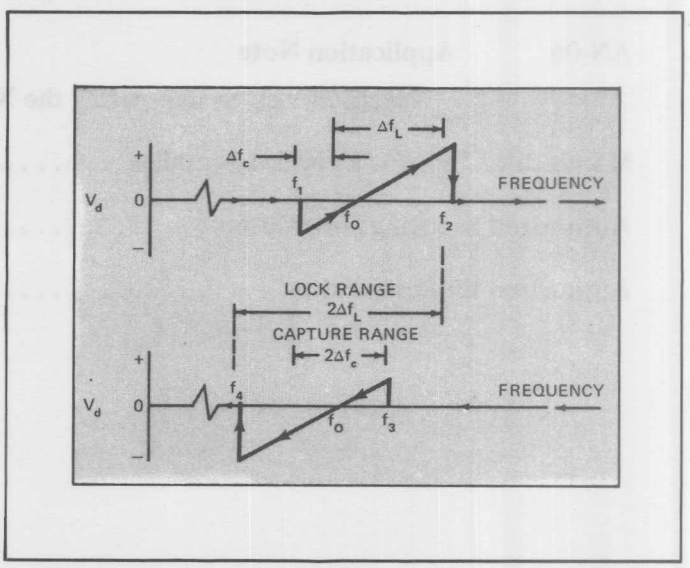


Figure 2. Typical PLL frequency-to-voltage transfer characteristics are shown for increasing (upper diagram) and decreasing (lower diagram) input frequency.

Applications of PLL IC's

The basic concept of the phase locked loop (PLL) has been around since the early 1930's and has been used for a variety of applications in instrumentation and space telemetry. However, before the advent of monolithic integration, cost and complexity considerations limited its use to precision measurements requiring very narrow bandwidths. In the past few years, the advantages of monolithic integration have changed the phase locked loop from a specialized design technique to a general-purpose building block. Therefore, what is "new" at this point is not the concept of the PLL, but its availability in a low-cost self contained monolithic IC package.

In many ways, this is similar to the case of the monolithic operational amplifier, which, until less than a decade ago, was an expensive building block. Today, with the advent of monolithic technology, it has become a basic building block in nearly every system design. The monolithic phase locked loop also offers a similar potential. In fact, many of the applications of the PLL outlined in this article become economically feasible only because the PLL is now available as a low-cost IC building block.

Today, over a dozen different integrated PLL products are available from a number of IC manufacturers. Some of these are designed as "general-purpose" circuits, suitable for a multitude of uses; others are intended or optimized for special applications such as tone detection, stereo decoding and frequency synthesis. This article is intended as a brief survey of the expanding field of monolithic phase locked loops. Its purpose is to familiarize the reader with their individual characteristics, capabilities and applications.

Applications for PLLs Abound

As a versatile building block, the PLL covers a wide range of applications. Some of the more important are the following:

FM demodulation: In this application, the PLL is locked on the input FM signal, and the loop-error voltage, $V_d(t)$ in Figure 1 (see Box), which keeps the VCO in lock with the input signal, represents the demodulated output. Since the system responds only to input signals within the capture range of the PLL, it also provides a high degree of frequency selectivity. In most applications, the quality of the demodulated output (i.e., its linearity and signal/noise ratio) obtained from a PLL is superior to that of a conventional discriminator.

FSK demodulation: Frequency-shift keyed (FSK) signals are commonly used to transmit digital information over telephone lines. In this type of modulation, the carrier signal is shifted between two discrete frequencies to encode the binary data. When the PLL is locked on the input signal, tracking the shifts in the input frequency, the error voltage in the loop, $V_d(t)$, converts the frequency shifts back to binary logic pulses.

Signal conditioning: When the PLL is locked on a noisy input signal, the VCO output duplicates the frequency of the desired input but greatly attenuates the noise, undesired sidebands and interference present at the input. It is also a tracking filter since it can track a slowly varying input frequency.

Frequency synthesis: The PLL can be used to generate new frequencies from a stable reference source by either frequency multiplication and division, or by frequency translation. Figure 3 shows a typical frequency multiplication and division circuit, using a PLL and two programmable counters. In this application, one of the counters is inserted between the VCO and phase comparator and effectively divides the VCO frequency by the counter's modulus N. When the system is in lock, the VCO output is related to the reference frequency, f_R, by the counter moduli M and N as:

$$f_o = (\frac{N}{M})\, f_R$$

By adding a multiplier and an additional low-pass filter to a PLL (Figure 4), one can form a frequency translation loop. In this application, the VCO output is shifted from the reference frequency, f_R, by an amount equal to the offset frequency, f_1, i.e., $f_o = (f_R + f_1)$.

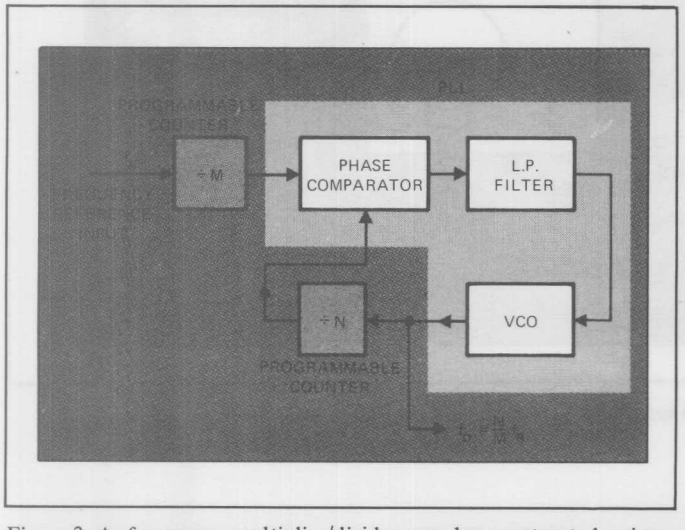


Figure 3. A frequency multiplier/divider can be constructed using a phase locked loop.

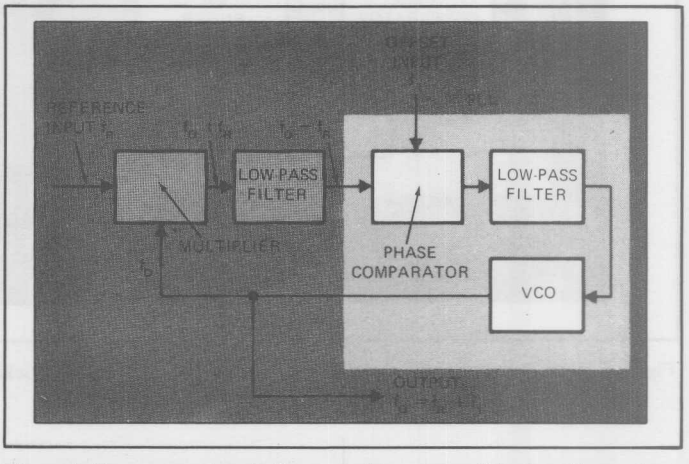


Figure 4. Frequency translation can be accomplished with a phase locked loop by adding a multiplier and an additional low-pass filter to the basic PLL.

Data synchronization: The PLL can be used to extract synchronization from a composite signal, or can be used to synchronize two data streams or system clocks to the same frequency reference. Such applications are useful in PCM data transmission, regenerative repeaters, CRT scanning and or drum memory read-write synchronization.

AM detection: The PLL can be converted to a synchronous AM detector with the addition of a non-critical phase-shift network, an analog multiplier and a low-pass filter. The system block diagram for this application is shown in Figure 5.

In this application, as the PLL tracks the carrier of the input signal, the VCO regenerates the unmodulated carrier and feeds it to the reference input of the multiplier section. In this manner, the system functions as a synchronous demodulator with the filtered output of the multiplier representing the demodulated audio information.

Tone detection: In this application, the PLL is again connected as shown in Figure 5. When a signal tone is present at the input, within a frequency band corresponding to the capture range of the PLL, the output dc voltage is shifted from its tone-absent level. This shift is easily converted to a logic signal by adding a threshold detector with logic-compatible output levels.

Motor speed control: Many electromechanical systems, such as magnetic tape drives and sick or drum head drivers, require precise speed control. This can be achieved using a PLL system, as shown in Figure 6. The VCO section of the monolithic PLL is separated from the phase-comparator and used to generate a voltage controlled reference frequency, f_R. The motor shaft and the tachometer output provide the second signal, frequency f_M, which is compared to the reference frequency. The controller is a power amplifier which drives the speed-control

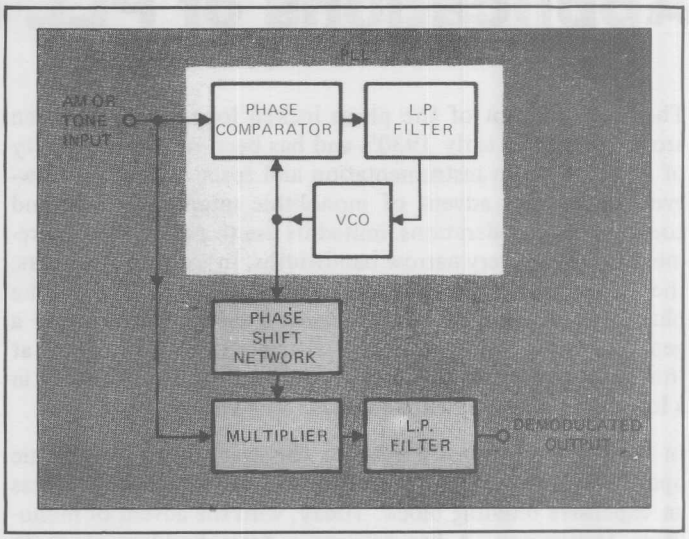


Figure 5. AM and tone detection are possible by adding three functional blocks to the basic phase locked loop.

windings of the motor. Thus, the motor and tachometer combination essentially functions as a VCO which is phase locked to the voltage controlled reference frequency, f_R.

Stereo decoding: In commercial FM broadcasting, suppressed carrier AM modulation is used to superimpose the stereo information on the FM signal. To demodulate the complex stereo signal, a low-level pilot tone is transmitted at 19 kHz (1/2 of actual carrier frequency). The PLL can be used to lock onto this pilot tone, and regenerate a coherent 38 kHz carrier which is then used to demodulate the complete stereo signal. A number of highly specialized monolithic circuits have been developed for this application. A typical example of monolithic stereo decoder circuits using the PLL principle is the XR-1310 stereo demodulator IC.

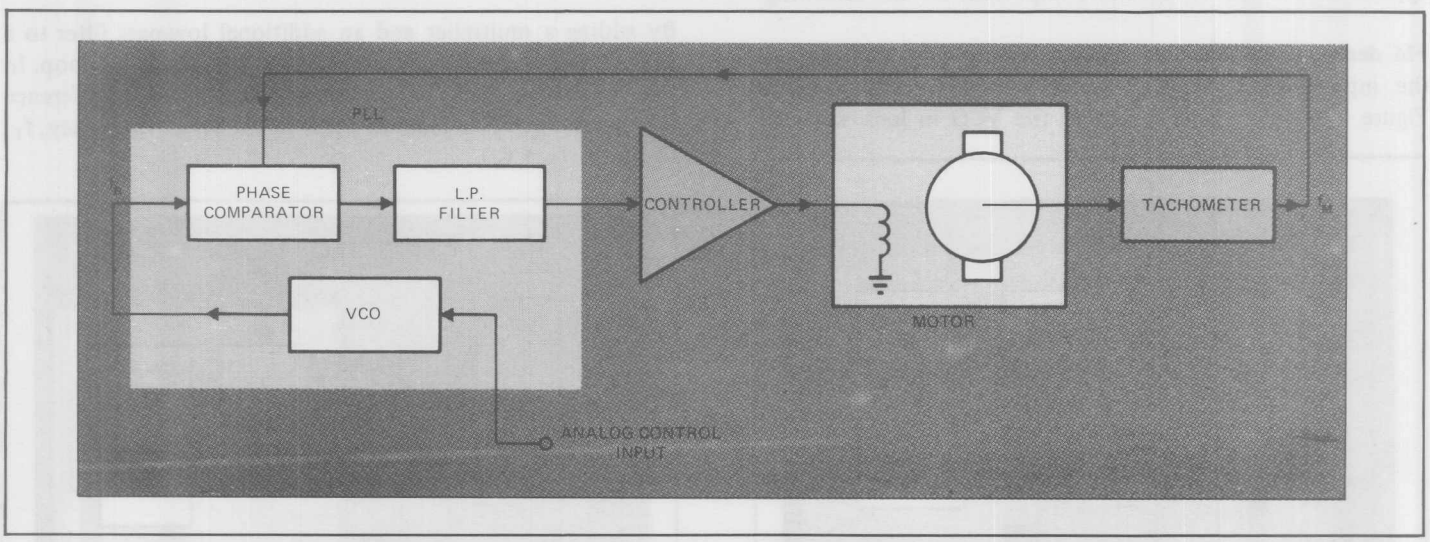


Figure 6. Very precise motor speed control is possible with a phase locked loop system of this type.

Overview of Exar's PLL Products

Exar offers the widest selection of monolithic phase-locked loop IC products in the industry. The purpose of this section is to familiarize the user with the key features and the characteristics of Exar's entire line of PLL products. Table 1 gives a comparative listing of the key features and characteristics of Exar's broad line of PLL products.

Exar's phase-locked loop products cover a wide range of applications and design approaches. In one extreme are the "uncommitted" or multi-function designs such as the XR-S200 and the XR-2212 which strive for maximum versatility by keeping each of the functional blocks on the chip independent of each other. Such devices are intended to serve as versatile building-blocks which can be tailored to many applications simply by the choice of external interconnections. On the other extreme are the "committed" special function devices, such as the XR-567 and the XR-2567 tone decoders which are optimized for tone detection applications. The key features of each of Exar's family of PLL products are briefly outlined below:

XR-S200 is a multi-function PLL containing a four-quadrant analog multiplier, a high-frequency VCO and an operational amplifier, and is housed in a 24-pin package. Each of the functional blocks and their control inputs are independent of each other. In other words, they can be externally connected in any order. Thus, it is essentially a custom, or do-it-yourself, PLL. The user determines the function and performance characteristics by his choice of external connections and components.

XR-210 was designed for FSK modulation/demodulation applications. In addition to the basic PLL, it contains a voltage comparator and a RS232-C compatible output logic driver. The VCO section can be used for FSK modulation and has independent mark/space adjustments.

XR-215 is a general-purpose PLL circuit particularly suited for FM demodulation, frequency synthesis, and tracking filter. The high-gain amplifier section can be used as an active filter, or can function as an audio preamplifier for FM detection. The VCO section has sweep and gain control options. A single PLL circuit can be time-multiplexed between two input channels by applying a binary input to its range-select control. The key feature of XR-215 is its high frequency capability (up to 35 MHz).

XR-2211 is an ultra-stable PLL system optimized for FSK MODEM design. It offers 20 ppm/°C VCO stability and an on-chip quadrative detector for tone or carrier-detect applications. Its tracking bandwidth can be controlled by choice of two external resistors.

XR-2212 is a versatile, precision PLL circuit with 20 ppm/°C oscillator stability. It is ideally suited for linear FM detection or frequency synthesis. The VCO section of the circuit is not internally connected to the phase-detector; thus, it can interface with an external TTL or MOS frequency divider for frequency synthesis applications.

XR-567 monolithic tone-decoder contains an internal current-controlled oscillator (CCO) and two separate phase-detectors driven from the same oscillator. The quadrature phase-detector, along with the buffer amplifier, is used to generate a binary output pulse if a signal tone at the input is within the pass-band of the system. Its detection bandwidth (capture range) and response time are controlled by external filter capacitors. It has high-current (100 mA) logic driver output.

XR-2567 dual tone-decoder system contains an equivalent of two independent 567 decoders on the same chip. It is particularly well suited for decoding multiple-tone inputs, such as those used in telephone dialing systems. Its operating voltage range is wider than that of the 567, and can switch two simultaneous 100 mA loads at the outputs. If only one of the two decoders is used, the remaining one can be deactivated to minimize power dissipation.

Table 1. A Summary of Exar's PLL Circuits

Product Designation	Package	Operating Supply Range	High Frequency Limit	VCO Stability		Primary Applications
				Power Supply (%/V)	Temp. (ppm/°C)	
XR-S200	24 Pin DIP	6V to 30V ±3V to ±15V	30 MHz	0.08 (typ) 0.5 (max)	300 (typ) 650 (max)	Multi-function building block for FM/FSK detection, frequency synthesis
XR-210	16 Pin DIP	5V to 26V	20 MHz	0.05 (typ) 0.5 (max)	200 (typ) 550 (max)	FSK modem, frequency synthesis, data synchronization
XR-215	16 Pin DIP	5V to 26V	35 MHz	0.1 (typ) 0.5 (max)	250 (typ) 600 (max)	General purpose PLL. FM demodulation tracking filter, frequency synthesis
XR-2211	15 Pin DIP	4.5V to 20V	300 kHz	0.05 (typ) 0.5 (max)	±20 (typ) ±50 (max)	FSK demodulation, tone decoding, carrier detection
XR-2212	16 Pin DIP	4.5V to 20V	300 kHz	0.05 (typ) 0.5 (max)	±20 (typ) ±50 (max)	Frequency synthesis, FM detection, data synchronization, tracking filter
XR-567	8 Pin DIP	4.75V to 9V	500 kHz	0.5 (typ) 1 (max)	±140 (typ)	Tone detection
XR-2567	16 Pin DIP	4.75V to 15V	600 kHz	0.05 (typ) 0.2 (max)	±100 (typ)	Dual tone decoder (Dual 567 equivalent)

Motor speed control: In most speed-control applications, a tachometer connected to the motor shaft is used as the VCO in the loop and the actual VCO on the monolithic chip is either not used or used to generate a reference frequency (see Figure 6). Thus, a PLL system which can be broken between the low-pass filter and the VCO is needed. The PLL IC most suited to this application is the XR-2212 because of its wide tracking range.

AM detection: This application requires an additional analog multiplier section to be added to the basic PLL (see Figure 3). The XR-2208 Operational Multiplier IC which contains a four-quadrant multiplier and an op. amp. on the same chip is ideally suited for this function. It can be used in conjunction with either the XR-215 or the XR-2212 PLL circuits to perform this function.

Table 2
Major Applications for Exar's PLL Circuits

MAJOR APPLICATION	PART NUMBER						
	XR-S200	XR-210	XR-215	XR-2211	XR-2212	XR-567	XR-2567
FM DEMODULATION							
HIGH FREQUENCY	✓	✓	✓				
LOW FREQUENCY			✓		✓		
FREQUENCY SYNTHESIS							
HIGH FREQUENCY	✓	✓	✓				
LOW FREQUENCY		✓	✓		✓		
FSK DEMODULATION		✓		✓			
SIGNAL CONDITIONING	✓				✓		
TONE DETECTION				✓		✓	✓
MOTOR SPEED CONTROL	✓				✓		
DATA SYNCHRONIZATION			✓		✓		

Choosing the Right PLL Circuit

At the onset of his design, the user of monolithic PLL products is faced with the key question of choosing the phase-locked loop IC best suited to his application. The broad line of PLL products offered by Exar cover a wide range of applications. It is often difficult to determine at a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question, "What is the best PLL product for the job?"

Table 2 gives a brief listing of some of the major classes of PLL applications, and lists the recommended circuits for each. A further discussion of the key performance parameters associated with each application are also listed below.

FM demodulation: Essentially all the PLL circuits listed in Table 1 can be used for FM demodulation. However, it is often possible to narrow the choice down to 2 or 3 circuits, based on the particular performance criteria. In general, there are three key performance parameters which should be examined:

- ☐ Quality of demodulated output: This is normally measured in terms of the output level, distortion, and signal/noise ratio for a given FM deviation.
- ☐ VCO frequency range and frequency stability: For reliable operation, VCO upper frequency limit (see Table 1) should be at least 20% above the FM carrier frequency. VCO frequency stability is important, especially if a narrow-band filter is used in front of the PLL, or multiple input channels are present. If the VCO exhibits excessive drift, the PLL can drift out of the input signal band as the ambient temperature varies.
- ☐ Detection threshold: This parameter determines minimum signal level necessary for the PLL to lock and demodulate an FM signal of given deviation.

In most FM demodulation applications, it is also desirable to control the amplitude of the demodulated output. This feature is provided in some of the PLL circuits (such as the XR-215 and the XR-2212) by means of a variable-gain amplifier contained on the chip.

For low-frequency FM detection (below 300 kHz carrier frequency) the XR-2212 is recommended because of its versatility and temperature stability. For FM demodulation at frequencies above 300 kHz, the XR-2215 offers the best performance because of its high frequency capability.

FSK decoding: Frequency-shift keying used in digital communications is very similar to analog FM modulation. Therefore, any PLL IC can be used for FSK decoding, provided that its input sensitivity and the tracking range are sufficient for a given FSK signal deviation. Some of the basic requirements and desirable features for a PLL used in FSK decoding are:

- ☐ Center frequency stability.
- ☐ Logic compatible output.
- ☐ Control of VCO conversion gain.

Center frequency stability is essential to insure that the VCO frequency range stays within the signal band over the operating temperature range. A logic compatible output is desirable to avoid the need for an external voltage comparator (slicer) to square the output pulses. It is particularly convenient if the output conforms to RS-232C standard, thereby eliminating the need for a separate line-driver circuit. Control of the VCO's conversion gain allows the circuit to be used for both large deviation FSK signals (such as 1200 baud operation) as well as for small deviation (75 baud) FSK signals.

For FSK decoding at low frequencies (i.e. below 300 kHz) the XR-2211 is by far the optimum circuit to use because of its frequency stability and carrier-detect capability. For FSK detection at higher frequencies (up to 10 MHz) the XR-210 is the recommended circuit.

Frequency synthesis: This application requires a PLL circuit with the loop opened between the VCO output and the phase comparator input, so that an external frequency divider can be inserted into the feedback loop of the PLL. This requirement is satisfied by XR-S200, XR-210, XR-215 and the XR-2212 PLL circuits.

For frequency synthesis at low frequencies (i.e. with maximum output frequency less than 300 kHz) the XR-2212 is by far the best suited circuit since it has the best VCO stability and interfaces easily with all logic families. For operation above 300 kHz, either the XR-210 or the XR-215 PLL IC's can be used for frequency synthesis; however the XR-215 offers the highest frequency capability.

Signal conditioning: Most signal conditioning applications require very narrow-band operation of the PLL. This in turn may require the use of active filters within the loop (between the phase detector and the VCO). The PLL circuits which allow active filters to be inserted into the loop are the XR-S200 and the XR-2212. Both of these circuits already contain an op. amp. on the chip for active filtering. For low frequencies (i.e. below 300 kHz) the XR-2212 is the best suited circuit because of its adjustable tracking bandwidth and excellent frequency stability. For higher frequencies the XR-S200 is the recommended circuit.

Tone decoding: The PLL circuits especially designed for this application are the XR-567, the XR-2567 and the XR-2211. The XR-2211 offers the highest frequency stability, and independent control of system bandwidth and response time, among the three circuits. The XR-567 has a relatively high input threshold ($\approx$ 20 mV, rms) and may require input preamplification; however it requires fewer external components than the XR-2211. The XR-2567, which contains two independent 567-type tone decoders on the same chip may be more economical to use in multiple-tone detection systems.

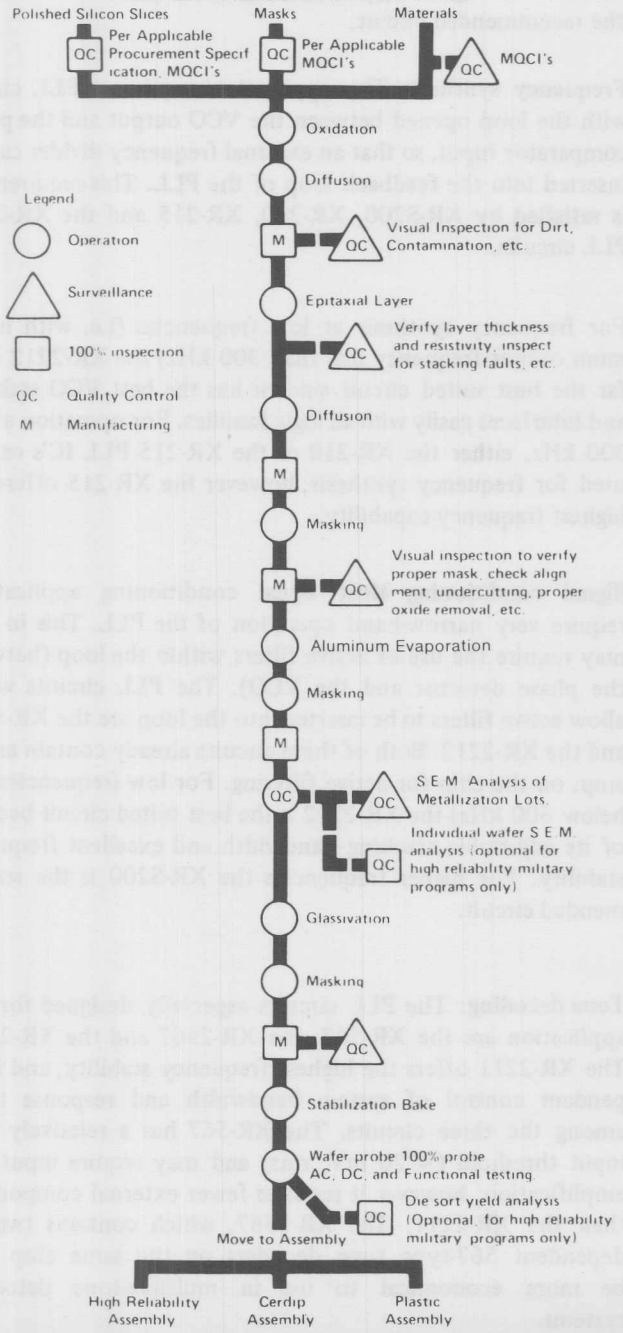
Quality Assurance Standards

The quality assurance program at Exar Integrated Systems defines and establishes standards and controls on manufacturing, and audits product quality at critical points during manufacturing. The accompanying Manufacturing/QA process flows illustrate where quality assurance audits, by inspection or test, the manufacturing process. The insertion of these quality assurance points is designed to insure the highest quality standards are maintained on Exar product during its manufacture.

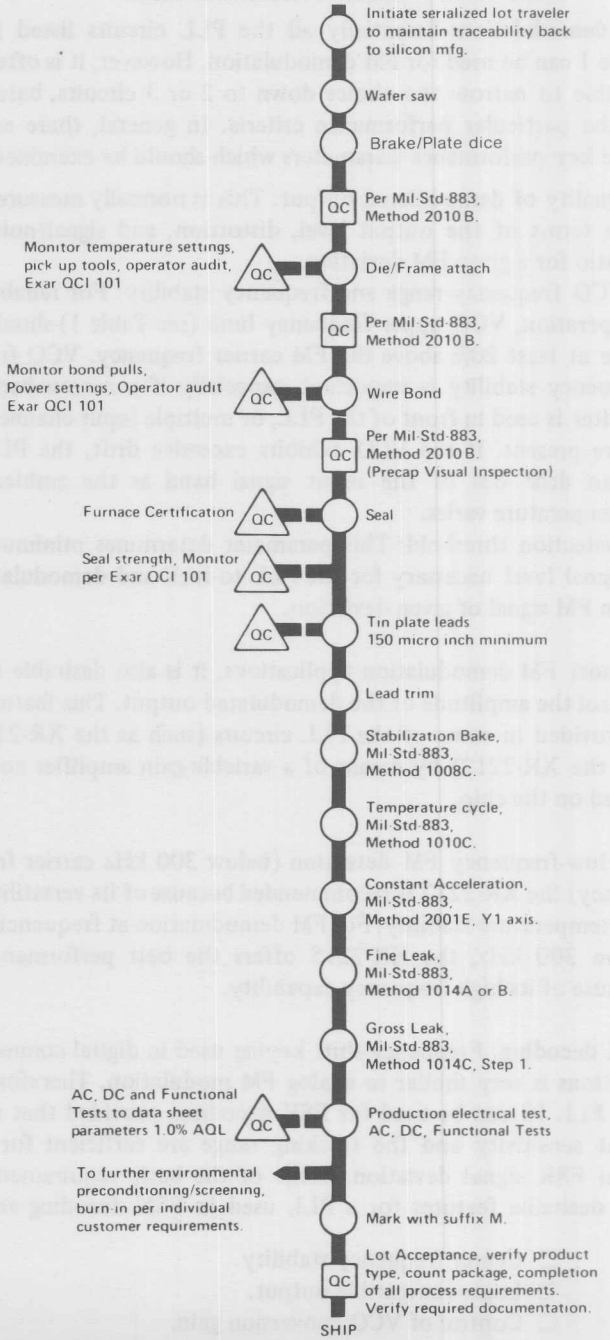
Realizing that these standard Manufacturing/QA process flows do not meet the needs of every customers specific requirements, Exar quality assurance can negotiate and will screen product to meet any individual customer's specific requirement.

All products ending with the suffix M are fully screened to the requirements of MIL-STD-883, Method 5004, Condition C.

WAFER FABRICATION/QA FLOW



HIGH RELIABILITY ASSEMBLY/QA FLOW



XR-S200

Multi-Function PLL System

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The XR-S200 integrated circuit is a highly versatile, multipurpose circuit that contains all of the essential functions of most communication system designs on a single monolithic substrate. The functions contained in the XR-S200 include:

(1) a four quadrant analog multiplier, (2) a high frequency voltage controlled oscillator (VCO) and

(3) a high performance operational amplifier.

The three functions (Figure 1) can be used independently, or directly interconnected in any order to perform a large number of complex circuit functions. from phase-locked loops to the generation of complex waveforms. The XR-S200 can accomodate both analog and digital signals, over a frequency range of 0.1 Hz to 30 MHz, and operate with a wide choice of power supplies extending from ±3 volts to ±30 volts.

TYPICAL APPLICATIONS OF THE XR-S200

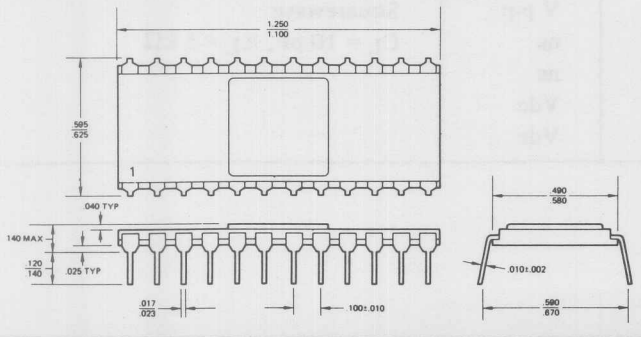
- Phase-locked loops
- FM demodulation
  - Narrow and wideband FM ■ Commercial FM-IF
  - TV sound and SCA detection
- FSK detection (MODEM)
- PSK demodulation
- Signal conditioning
- Tracking filters
- Frequency synthesis
- Telemetry coding/decoding
- AM detection
  - Quadrature detectors ■ Synchronous detectors
- Linear sweep & FM generation
  - Crystal controlled ■ Suppressed carrier
  - Double sideband
- Tone generation/detection
- Waveform generation
  - Single/square/triangle/sawtooth
- Analog multiplication

ABSOLUTE MAXIMUM RATINGS

Power Supply	30 volts
Power Dissipation	900 mW
Derate above +25°C	5 mW/°C
Temperature	
Operating	−55°C to +125°C
Storage	−65°C to +150°C
Input Signal Level, V_S	6 V,p-p

PACKAGE OUTLINE

24 Pin Dual-In-Line Metal Ceramic Package



SYSTEM BLOCK DIAGRAM

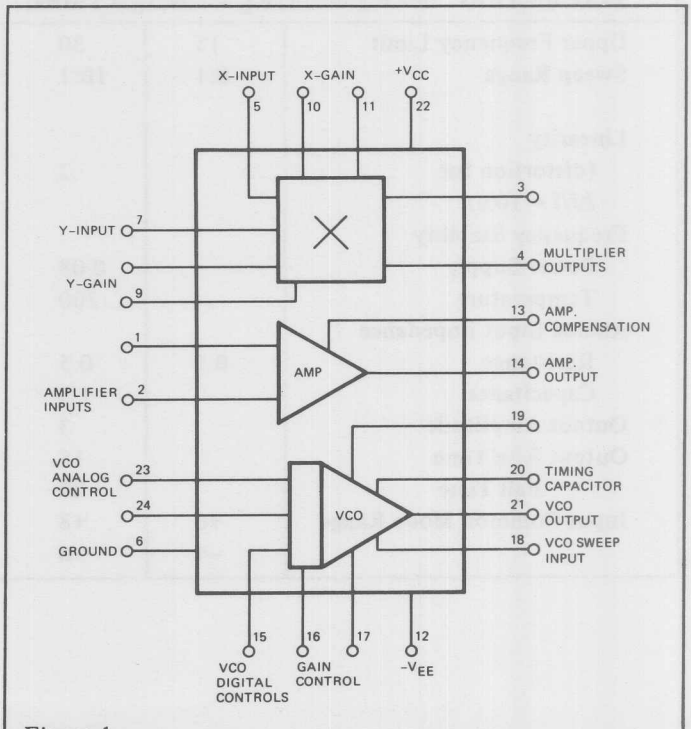


Figure 1.

ELECTRICAL SPECIFICATIONS ($T = 25°C$, $V_{SUPPLY} = \pm 10V$)

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
MULTIPLIER SECTION: See Figure 2, $R_X = R_Y = 15k$, Pins 1, 2, 6, 23, 24 Grounded.					
Output Offset Voltage		±40	±120	mV	$V_X = V_Y = 0$, $V_{IO} = \lvert V_3 - V_4 \rvert$
Input Bias Current		5	15	μA	Measured at pins 5 and 7
Input Offset Current		0.1	1.0	μA	Measured at pins 5 and 7
Linearity					
(Output error, %		1.0		%	$-5 < V_X < +5$, $V_Y = \pm 5V$
of full scale)		1.5		%	$-5 < V_Y < +5$, $V_X = \pm 5V$
Scale Factor, K_M		0.1		–	$K_M = 25/R_X R_Y$ (Adjustable)
Input Resistance	0.3	1.0		MΩ	f = 20 Hz, Measured at pins 5 and 7
3 dB Bandwidth	3	6		MHz	$C_L \leq 5$ pF
Phase detection B.W.	50	100		MHz	$R_X = R_Y = 0$
Differential Output Swing	±4	±6		V p-p	Measured across pins 3 and 4
Output Impedance					
Single Ended		6		kΩ	Measured at pins 3 and 4
Differential		12		kΩ	
OPERATIONAL AMPLIFIER SECTION: (See Figure 10 and 11, $R_L = 20k$, $C_L = 550$ pF.					
Input Bias Current		0.08	0.5	μA	
Input Offset Current		0.02	0.2	μA	
Input Offset Voltage		1.0	6.0	mVdc	
Differential Input Impedance					Open loop, f = 20 Hz
Resistance	0.4	2.0		MΩ	
Capacitance		1.0		pF	
Common Mode Range		±8		V	
Common Mode Rejection	70	90		dB	f = 20 Hz
Open Loop Voltage Gain	66	80		dB	
Output Impedance		2		kΩ	
Output Voltage Swing	±7	±9		V	$R_L \geq 20$ kΩ
Power Supply Sensitivity		30		μV/V	$R_S \leq 10$ kΩ
Slew Rate		2.5		V/μsec	$A_V = 1$, $C_L = 10$ pF
VCO SECTION: See Figure 11, $R_L = 10k$, $f_O = 1$ MHz.					
Upper Frequency Limit	15	30		MHz	$C_O = 10$ pF
Sweep Range	8:1	10:1		–	$f_O = 10$ kHz, See Figure 14
					Digital Controls Off
Linearity					
(distortion for		.2	1.0	%	Digital Controls Off
$\Delta f/f = 10\%$)					
Frequency Stability					$V_{CC} > 8V$, $f_O = 1$ MHz
Power Supply		0.08	0.5	%/V	Sweep Input Open
Temperature		300	650	ppm/°C	
Analog Input Impedance					Measured at pins 23 and 24
Resistance	0.1	0.5		MΩ	
Capacitance		1.5		pF	
Output Amplitude		3		V p-p	Squarewave
Output Rise Time		15		ns	$C_L = 10$ pF, $R_L = 5$ kΩ
Fall Time		20		ns	
Input Common Mode Range	+6	+8		Vdc	
	–4	–6		Vdc	

XR-S200 ANALOG MULTIPLIER SECTION

The analog multiplier in the XR-S200 (Figure 2) provides linear four-quadrant multiplication over a broad range of input signal levels. It also serves as a balanced modulator, phase comparator, or synchronous detector. Gain is externally adjustable. Nonlinearity is less than 2% of full scale output.

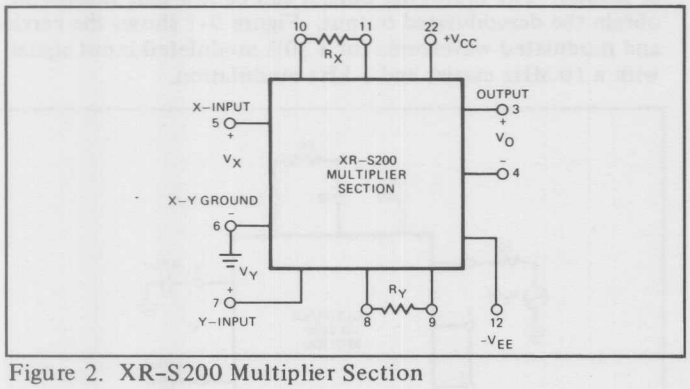


Figure 2. XR-S200 Multiplier Section

TYPICAL APPLICATIONS OF MULTIPLIER SECTION

- Analog multiplication/division
- Phase detection
- Balanced modulation/demodulation
- Electronic gain control
- Synchronous detection
- Frequency doubling

ANALOG MULTIPLICATION

The XR-S200 multiplier section can be combined with the amplifier section to perform analog multiplication without the need for dc level shifting between input and output. The amplifier functions as an operational amplifier with a single-ended output at ground level when connected as shown in Figure 3.

PHASE COMPARATOR

For phase comparison, a low-level reference signal is normally applied to one input and a high-level reference or carrier signal to the other input, as in Figure 4. The signal may be applied to either the X or Y input, since the response is symmetrical.

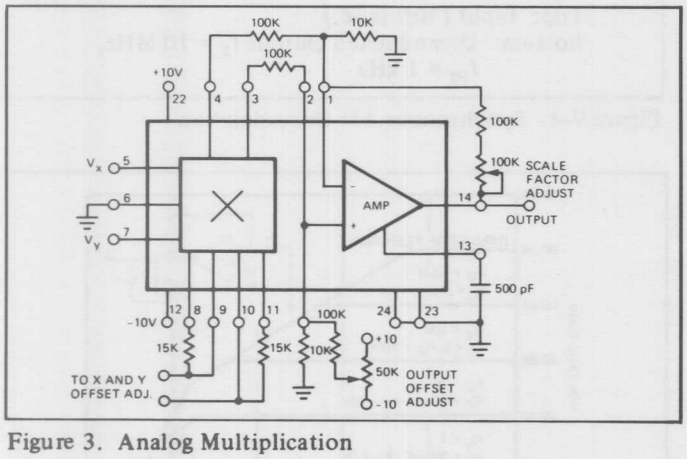


Figure 3. Analog Multiplication

If the two inputs, $V_R(t)$ and $V_S(t)$ are at the same frequency, then the dc voltage at the output of the phase comparator can be related to the phase angle ϕ between the two signals as

$$V_\phi = K_\phi \cos\phi$$

where K_ϕ is the conversion gain in volts per radian (Figure 5). For phase comparator applications, one input is normally a high level reference signal and the other input a low level

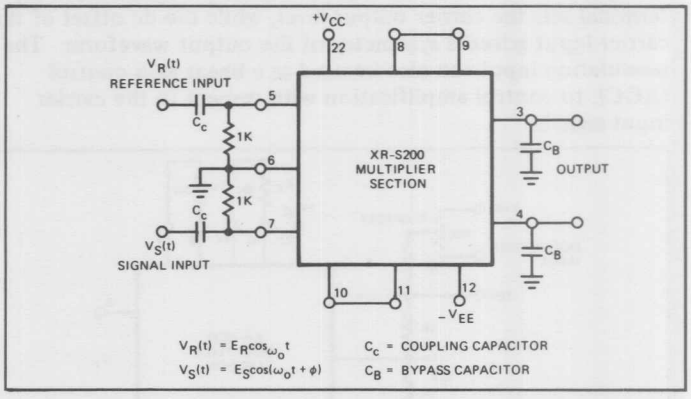


Figure 4. XR-S200 Multiplier Section as a Phase Comparator

information signal. Since the XR-S200 multiplier section offers symmetrical response with respect to the X and Y inputs, either input can be used as the carrier or signal input. For low input levels, the conversion gain is proportional to the input signal amplitude. For high level inputs, (V_S> 40 mV, rms) K_ϕ is constant and approximately equal to 2V/rad.

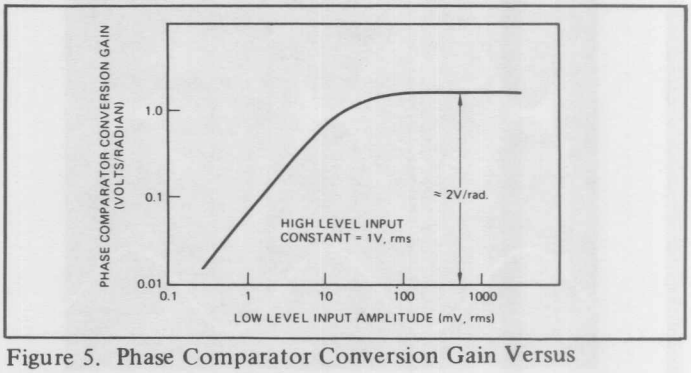


Figure 5. Phase Comparator Conversion Gain Versus Input Amplitude

SUPPRESSED-CARRIER AM

The multiplier generates suppressed-carrier AM signals when connected as in Figure 6. Again, the symmetrical response allows the X or Y inputs to be used interchangeably as the carrier or modulation inputs. The X and Y offset adjustments optimize carrier suppression. Gain control resistors R_X and R_Y typically range from 1 KΩ to 10 KΩ, depending on input signal amplitudes. The values shown give approximately 60 dB carrier suppression at 500 kHz and 40 dB at 10 MHz.

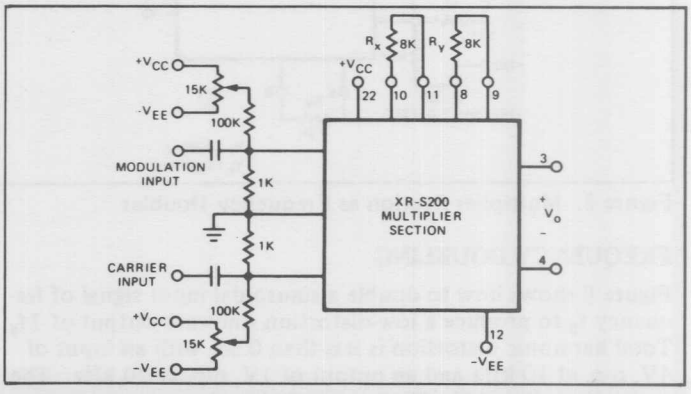


Figure 6. Suppressed Carrier Modulation Using XR-S200 Multiplier Section

DOUBLE-SIDEBAND AM GENERATION

The connection for double-sideband AM generation is shown in Figure 7. The dc offset adjustment on the modulation input terminal sets the carrier output level, while the dc offset of the carrier input governs symmetry of the output waveform. The modulation input can also be used as a linear gain control (AGC), to control amplification with respect to the carrier input signals.

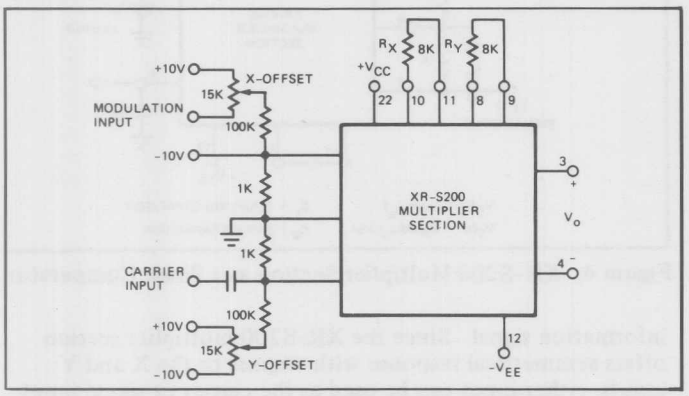


Figure 7. Double Sideband Amplitude Modulation Using XR-S200 Multiplier Section

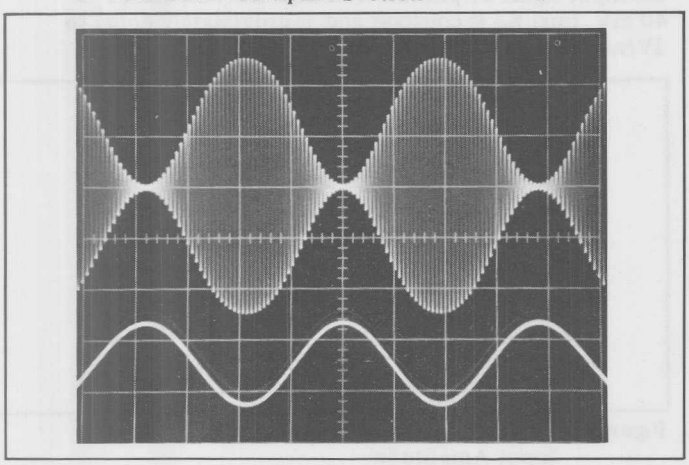


Figure 7-1. AM Modulation, 95% AM, f_C = 50 kHz, f_m = 1 kHz

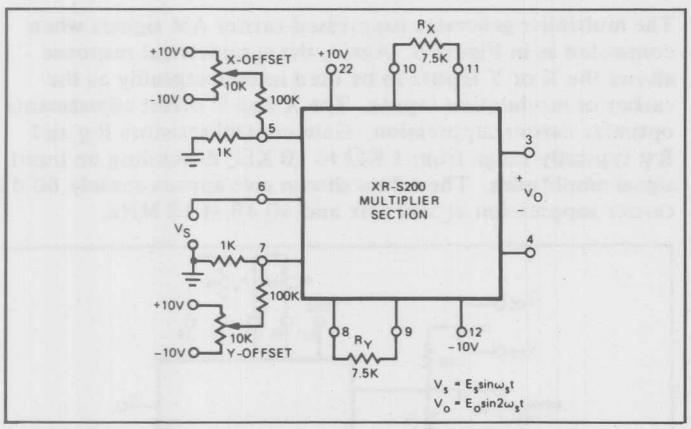


Figure 8. Multiplier Section as Frequency Doubler

FREQUENCY DOUBLING

Figure 8 shows how to double a sinusoidal input signal of frequency f_S to produce a low-distortion sinewave output of $2f_S$. Total harmonic distortion is less than 0.6% with an input of 4V, p-p, at 10 kHz and an output of 1V, p-p, at 20 kHz. The multiplier's X and Y offsets are nulled as shown to minimize the output's harmonic content.

SYNCHRONOUS AM DETECTION

A typical synchronous AM detector is shown in Figure 9. The signal is applied to the multiplier common input and the X and Y inputs are grounded. Since the Y input operates at maximum gain with $R_Y = 0$, the detector gain and demodulated output linearity are determined by R_X. An R_X range of 1 KΩ to 10 KΩ is recommended for carrier amplitudes of 100 mV, p-p, or greater. The multiplier output can be low-pass filtered to obtain the demodulated output. Figure 9-1 shows the carrier and modulated waveforms for a 30% modulated input signal with a 10 MHz carrier and 1 kHz modulation.

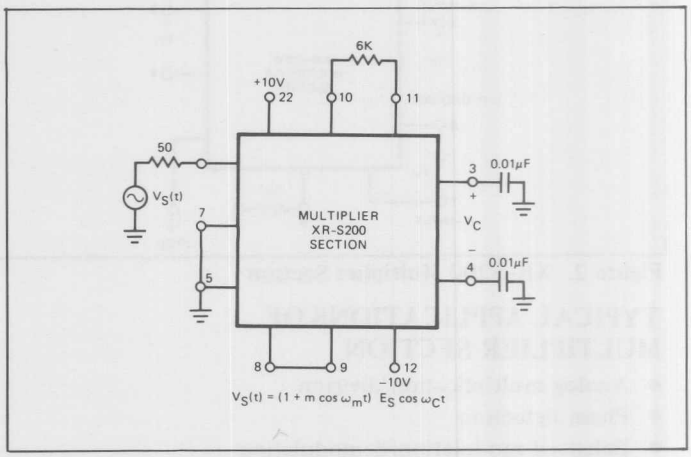
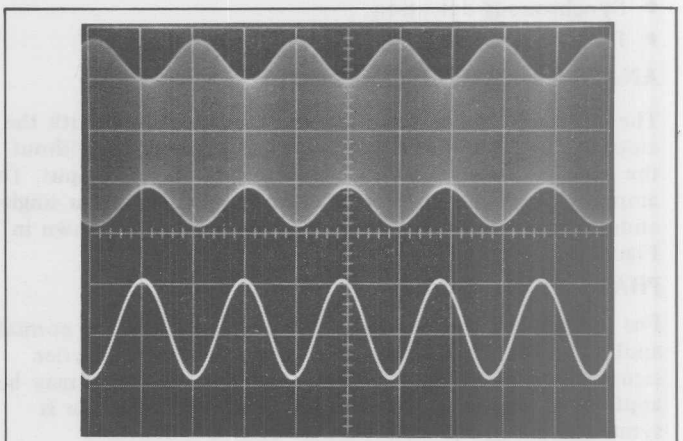


Figure 9. Synchronous AM Detector



Top: Input (30% mod.)
Bottom: Demodulated Output f_C = 10 MHz, f_m = 1 kHz

Figure 9-1. Synchronous AM Demodulation

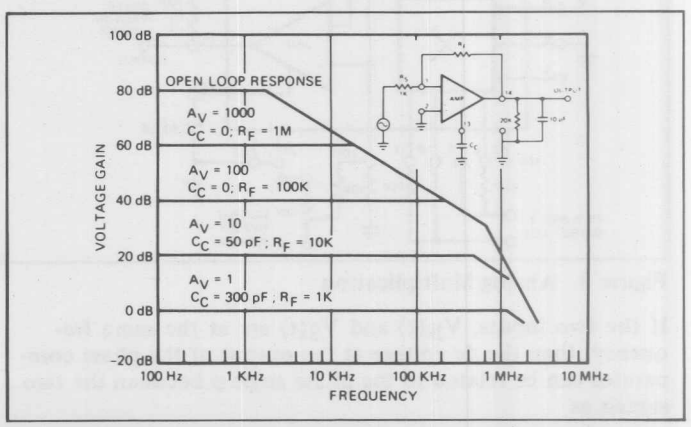


Figure 10. Amplifier Section Frequency Response

XR-S200 AMPLIFIER SECTION

This multi-purpose function (Figure 10) can be used as a general-purpose operational amplifier, high-speed comparator, or sense amplifier. It features an input impedance of 2 megohms, high voltage gain, and a slew rate of 2.5V/microsecond. The frequency response curves for the amplifier section are also shown in Figure 10.

XR-S200 OSCILLATOR SECTION

The voltage-controlled oscillator section, (Figure 11) is an exceptionally versatile design capable of operating from a fraction of a cycle to in excess of 40 MHz. Frequencies can be selected and controlled by three methods, and used in various combinations for different applications:

1. External timing capacitor C_0 tunes the VCO to a center frequency between 0.1 Hz and 40 MHz. The free-running frequency is inversely proportional to C_0. (see Figure 12)
2. Two digital control inputs allow four discrete frequencies to be selected at any center frequency. The digital inputs convert the logic signal voltages to internal control currents. (see Figure 13)
3. A sweep voltage, applied through a limiting resistor R_S is used for frequency sweeping, on-off keying, and synchronization of the VCO to a sync pulse. (see Figure 14)

The voltage-to-frequency conversion of the VCO section is highly linear. In addition, the conversion gain can be controlled through the analog control input. Gain is inversely proportional to R_O. When the digital controls are also used, gain decreases as the frequency is stepped up.

The VCO interfaces easily with ECL or TTL logic. It can be converted to a highly stable crystal-controlled oscillator by simply substituting a crystal in place of the timing capacitor, C_0.

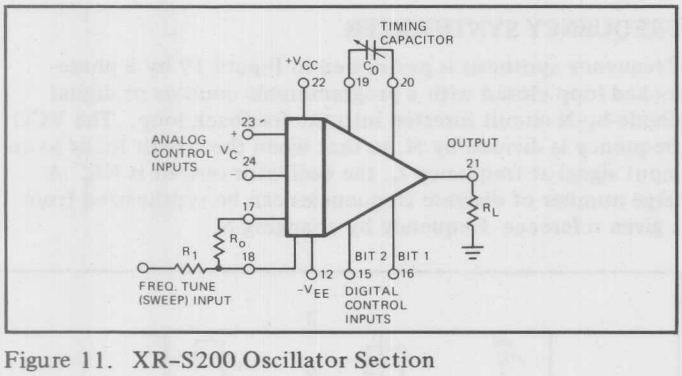


Figure 11. XR-S200 Oscillator Section

Typical performance characteristics of the VCO section are shown in Figures 12, 13, and 14.

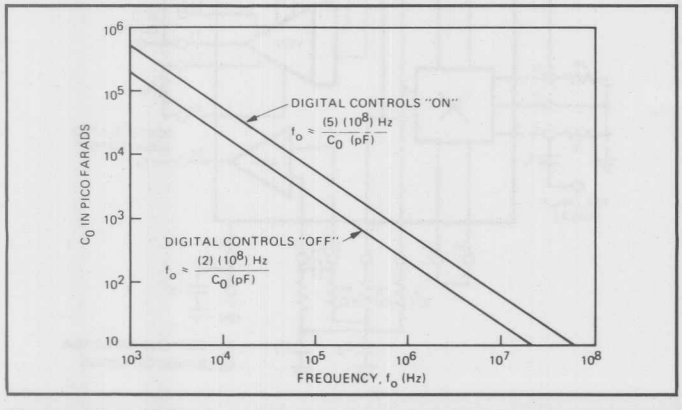


Figure 12. VCO Frequency as a Function of Timing Capacitor, C_0

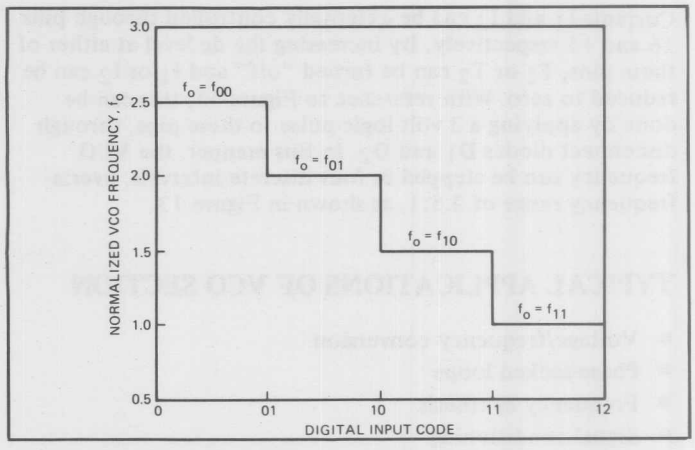


Figure 13. VCO Digital Tuning Characteristics

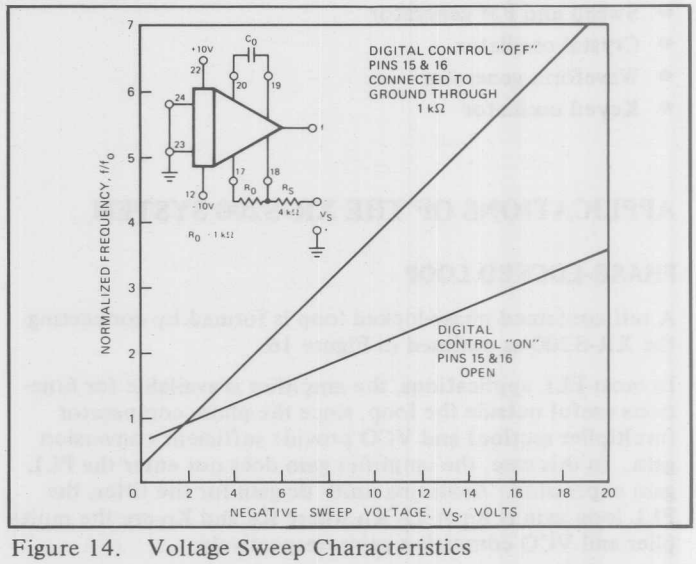


Figure 14. Voltage Sweep Characteristics

EXPLANATION OF VCO DIGITAL CONTROLS

The VCO frequency is proportional to the total charging current, I_T, applied to the timing capacitor. As shown in Figure 15, I_T is comprised of three separate components: I_0, I_1, and I_2, which are contributed by transistors T_0, T_1, and T_2, respectively. With pins 15 and 16 open circuited, these currents are interrelated as

$$I_0 = I_1 = 2I_2$$

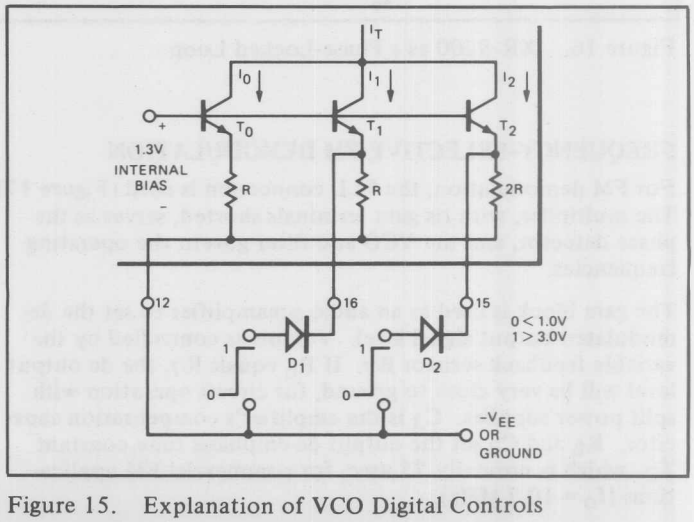


Figure 15. Explanation of VCO Digital Controls

Currents I_1 and I_2 cna be externally controlled through pins 16 and 15 respectively. By increasing the dc level at either of these pins, T_1 or T_2 can be turned "off" and I_1 or I_2 can be reduced to zero. With reference to Figure 15, this can be done by applying a 3 volt logic pulse to these pins, through disconnect diodes D_1 and D_2. In this manner, the VCO frequency can be stepped in four discrete intervals, over a frequency range of 2.5:1, as shown in Figure 13.

TYPICAL APPLICATIONS OF VCO SECTION

- Voltage/frequency conversion
- Phase-locked loops
- Frequency synthesis
- Signal conditioning
- Carrier generation
- Synchronization
- Sweep and FM generator
- Crystal oscillator
- Waveform generator
- Keyed oscillator

APPLICATIONS OF THE XR-S200 SYSTEM

PHASE-LOCKED LOOP

A self contained phase-locked loop is formed by connecting the XR-S200 as outlined in Figure 16.

In most PLL applications, the amplifier is available for functions useful outside the loop, since the phase comparator (multiplier section) and VCO provide sufficient conversion gain. In this case, the amplifier gain does not enter the PLL gain expression. Assuming unity dc gain for the filter, the PLL loop gain is $K_T = K_\phi K_0$ where K_ϕ and K_0 are the multiplier and VCO conversion gains, respectively.

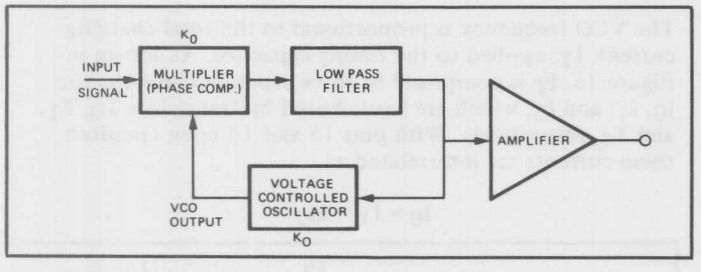


Figure 16. XR-S200 as a Phase-Locked Loop

FREQUENCY-SELECTIVE FM DEMODULATION

For FM demodulation, the PLL connection is used (Figure 17.) The multiplier, with its gain terminals shorted, serves as the phase detector, and the VCO and filter govern the operating frequencies.

The gain block is used as an audio preamplifier to set the demodulated output signal level. Volume is controlled by the variable feedback resistor R_7. If R_6 equals R_7, the dc output level will be very close to ground, for circuit operation with split power supplies. C_3 is the amplifier's compensation capacitor. R_8 and C_2 set the output de-emphasis time constant T_D, which is normally 75 μsec. for commercial FM applications (f_o = 10.7 MHz).

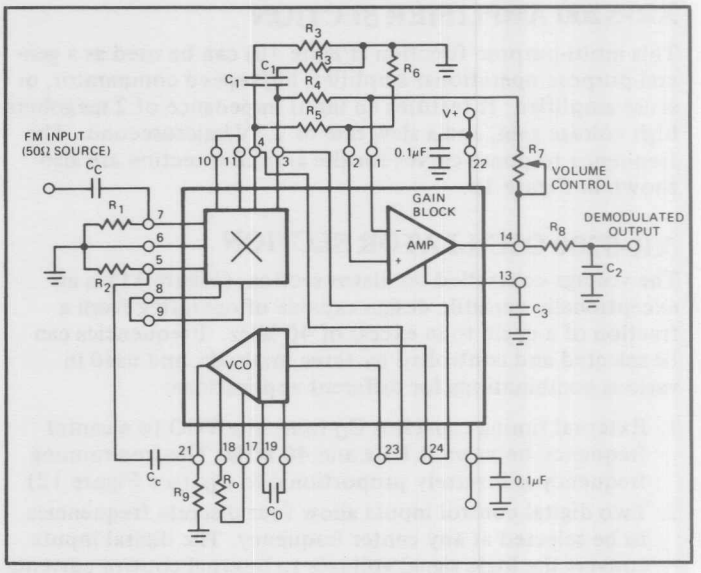


Figure 17. Circuit Connection for FM Detection

FSK DETECTION

FSK signals are detected and demodulated with the PLL connection, as well. It is shown in Figure 18 as a monolithic MODEM suitable for Bell 103 or 202 type data sets operating at data rates to 1800 baud. An input frequency shift corresponding to a data bit causes the multiplier's dc voltage output to reverse polarity. The dc level is changed to a binary output pulse by the gain block, connected as a voltage comparator.

FREQUENCY SYNTHESIZER

Frequency synthesis is performed in Figure 19 by a phase-locked loop closed with a programmable counter or digital divide-by-N circuit inserted into the feedback loop. The VCO frequency is divided by N, so that when the circuit locks to an input signal at frequency f_S, the oscillator output is Nf_S. A large number of discrete frequencies can be synthesized from a given reference frequency by changing N.

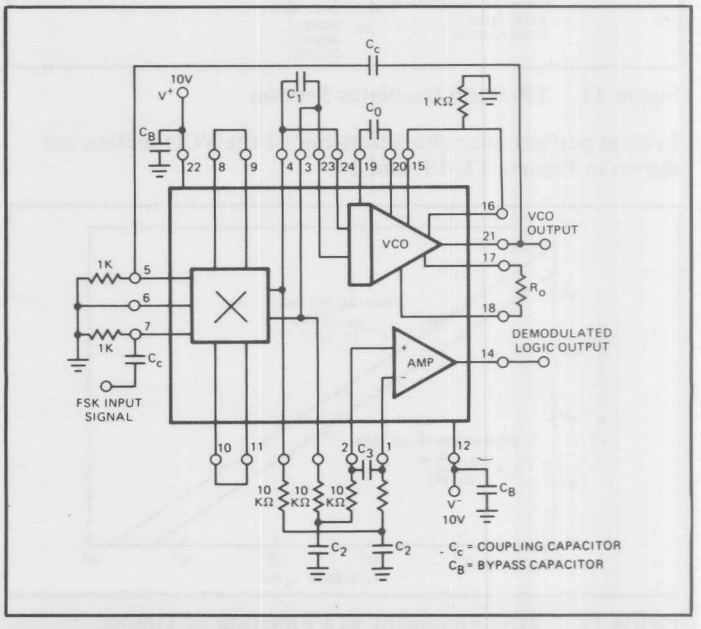


Figure 18. FSK Detection

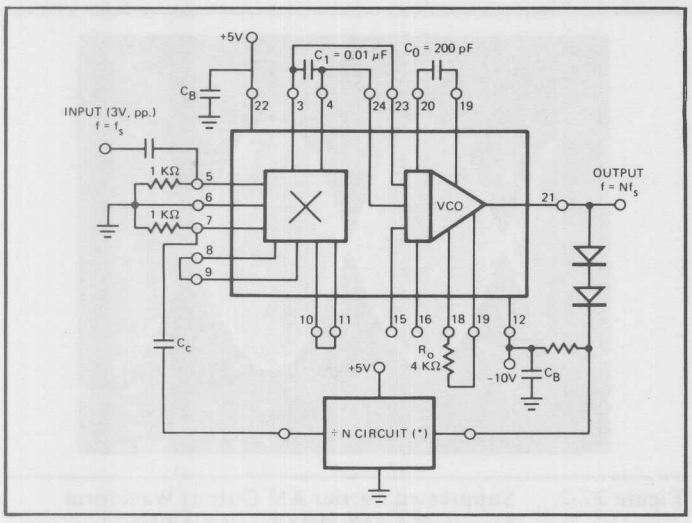


Figure 19. Frequency Synthesizer

The output frequency can be swept or frequency modulated by applying the proper analog control input to the circuit. For linear FM modulation with relatively small frequency deviation ($\Delta f/f < 10\%$) the modulation input can be applied across terminals 23 and 24. For large deviation sweep inputs, a negative going sweep voltage, V_S, can be applied to pin 18.

This allows the frequency to be voltage-tuned over approximately a 10:1 range in frequency. The digital control inputs (15 and 16) can be used for frequency-shift-keying (FSK) applications. They can be disabled by connecting them to ground through a current-limiting resistor.

AM & FM SIGNAL GENERATION

The oscillator and multiplier sections can be interconnected as a general purpose radio-frequency signal generator with AM,FM and sweep capability as shown in Figure 22.

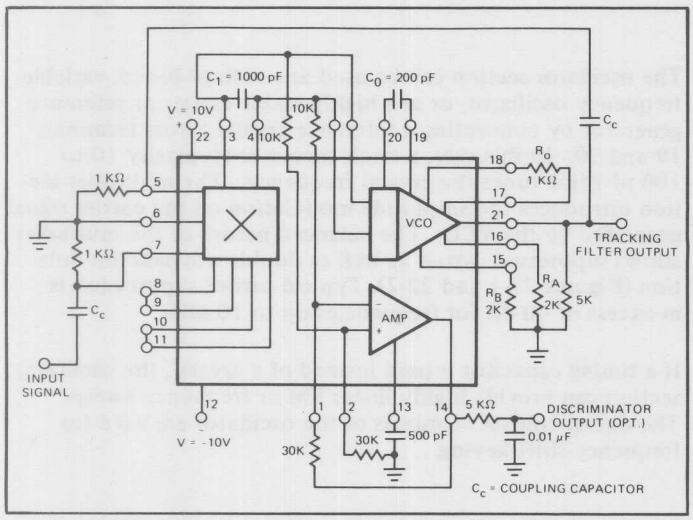


Figure 20. Recommended Circuit Connection for Tracking Filter Application (f_O = 1 MHz)

TRACKING FILTER AND WIDEBAND DISCRIMINATOR

In tracking filter applications, the XR-S200 again forms a PLL system (Figure 20). When the PLL locks on an input signal, it functions as a "frequency-filter" and produces a filtered version of the input signal frequency at the VCO output. Since it can track the input over a broad range of frequencies around the VCO free-running frequency, it is also called a "tracking filter". The system can track input signals over a 3:1 frequency range.

WAVEFORM GENERATOR

The XR-S200 can also be interconnected to form a versatile waveform generator. The typical circuit shown in Figure 21 generates the basic periodic square (or sawtooth) waveform. The multiplier section, connected as a linear differential amplifier, converts the differential sawtooth waveform input into a triangle wave output at pins 3 and 4. The waveform adjustment pot across pins 8 and 9 can be used to round the peaks of the triangle waveform and convert it to a low distortion sinewave (THD<2%). Terminals 3 and 4 can be used either differentially or single endedly to provide both in-phase and out-of-phase output waveforms.

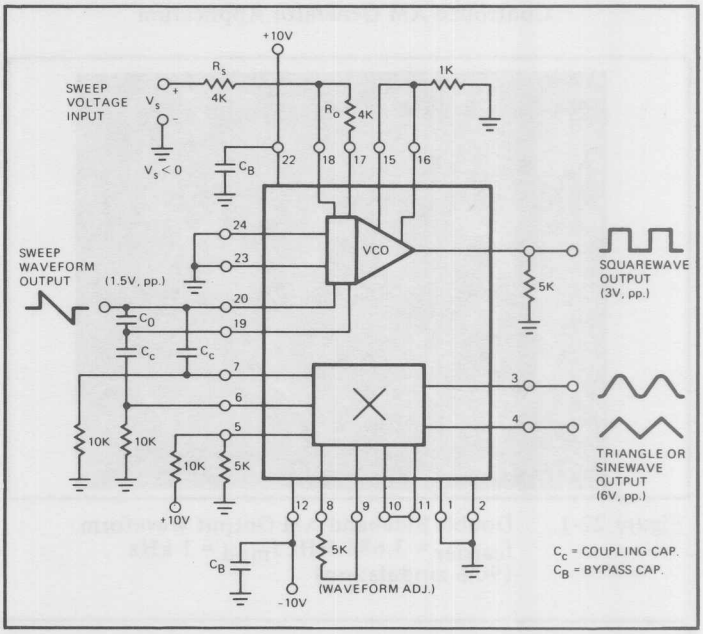


Figure 21. Waveform Generator Typical Circuit Connection Diagram

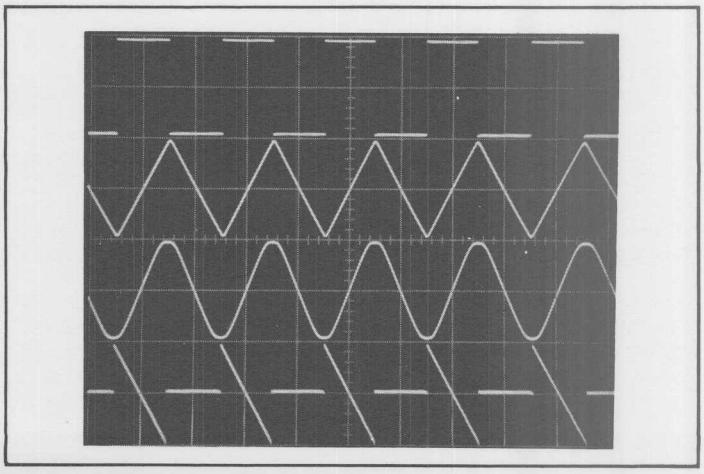


Figure 21-1. Basic Waveforms Available from XR-S200

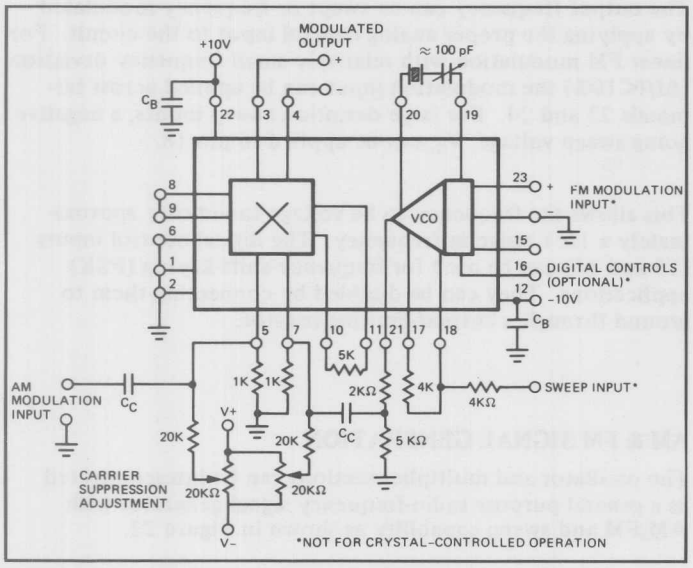


Figure 22. Circuit Connection for AM/FM or Crystal-Controlled AM Generator Application

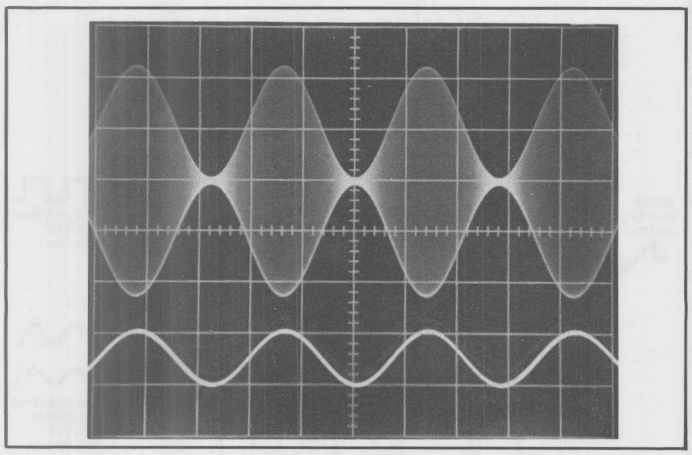


Figure 22-1. Double Sideband AM Output Waveform $f_{carrier}$ = 3.688 MHz f_{mod} = 1 kHz (90% modulation)

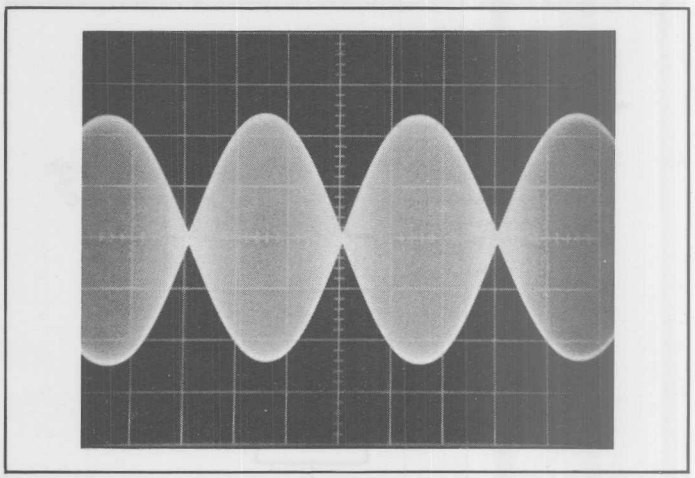


Figure 22-2. Suppressed Carrier AM Output Waveform $f_{carrier}$ = 3.688 MHz f_{mod} = 1 kHz

The oscillator section can be used as a voltage-tuned, variable frequency oscillator, or as a highly stable carrier or reference generator by connecting a reference crystal across terminals 19 and 20. In this case, a small capacitor (typically 10 to 100 pF) fine tunes the crystal frequency. The multiplier section introduces the amplitude modulation on the carrier signal generated by the VCO. The balanced nature of the multiplier allows suppressed carrier as well as double sideband modulation (Figures 22-1 and 22-2). Typical carrier suppression is in excess of 40 dB for frequencies up to 10 MHz.

If a timing capacitor is used instead of a crystal, the oscillator section can provide highly linear FM or frequency sweep. The digital control terminals of the oscillator are used for frequency-shift-keying.

XR-210

FSK Modulator/Demodulator

MAY 1977

The XR-210 is a highly versatile monolithic phase-locked loop system especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, as well as for frequency synthesis, tracking filters and tone decoding. The XR-210 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 20 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

FEATURES

Wide Frequency Range: 0.5 Hz to 20 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
RS-232C Compatible Demod. Output
DTL, TTL and ECL Logic Compatibility
Wide Dynamic Range: 300 μV to 3V
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to ±50%
Good Temperature Stability (200 ppm/°C)
High-Current Logic Output (50 mA)
Independent "Mark" and "Space" Frequency Adjustment
VCO Duty Cycle Control

APPLICATIONS

FSK Demodulation
FSK Generation
Data Synchronization
Frequency Synthesis
FM and Sweep Generation
Tracking Filter
Signal Conditioning
Tone Decoding
FM Detection
Wideband Discrimination
Voltage-to-Frequency Conversion

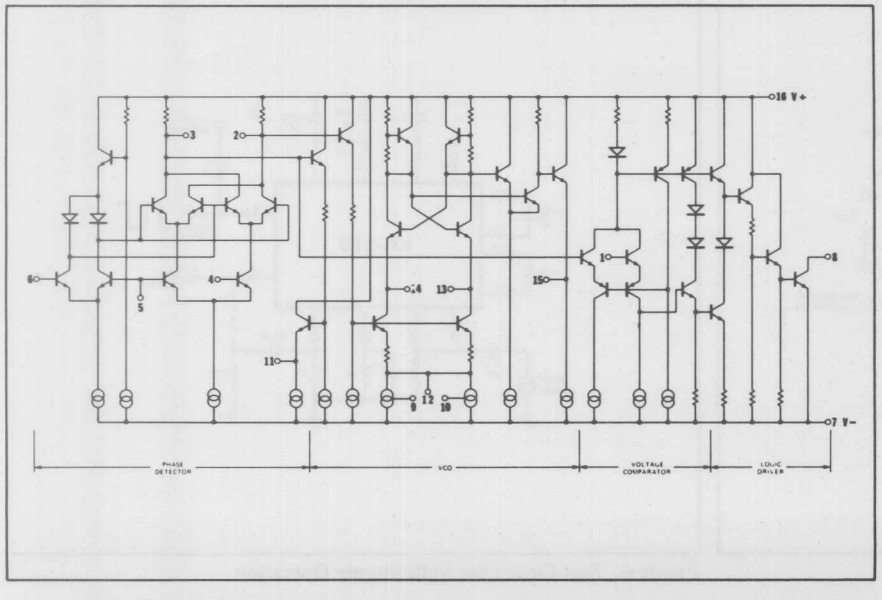
ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate above +25°C	6.0 mW/°C
Temperature	
Storage	−65°C to +150°C

AVAILABLE TYPES

Part Number	Package Types	Operating Temperature Range
XR-210M	Ceramic	−55°C to +125°C
XR-210	Ceramic	0°C to +75°C

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

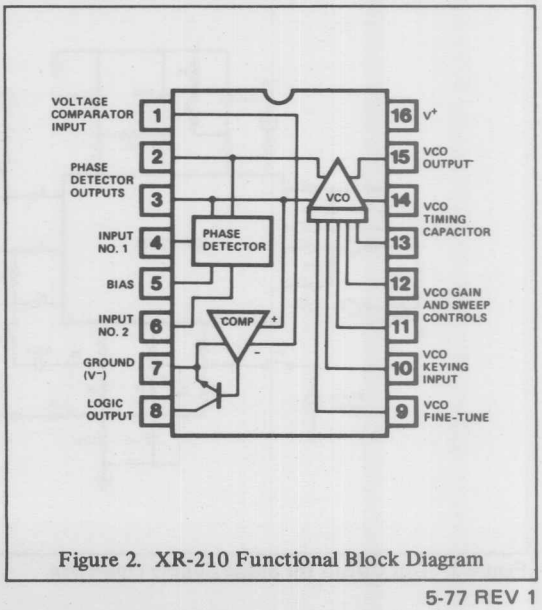


Figure 2. XR-210 Functional Block Diagram

5-77 REV 1

ELECTRICAL SPECIFICATIONS

Test Conditions: $V^+ = 12V$ (single supply), $T_A = 25°C$, Test circuit of Figure 3 with $C_0 = 0.02\ \mu F$, S_1, S_2, S_5 closed, S_3, S_4, S_6, S_7 open, unless otherwise specified.

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
Supply Voltage					
Single Supply	5		26	V dc	See Figure 3
Split Supply	±2.5		±13	V dc	See Figure 4
Supply Current	9	12	16	mA	See Figure 3, S_2 open
Upper Frequency Limit	15	20		MHz	See Figure 3, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	$C_0 = 500\ \mu F$
VCO Section					
Stability					
Temperature		200	550	ppm/°C	f = 10 kHz, $V^+ \geq 10V$, $0 < T_A < 75°C$
Power Supply		0.05	0.5	%/V	$10V < V^+ < 24V$
Sweep Range	5:1	8:1			S_3 closed, S_4 open, $0 < V_S < 6V$ See Figure 7, $V^+ = 12V$
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Duty Cycle Asymmetry		±1	±3	%	S_5 open
Rise Time		20		ns	10 pF to ground at Pin 15, S_5 open
Fall Time		40		ns	10 pF to ground at Pin 15, S_5 open
Phase Detector Section					
Conversion Gain		2		V/rad	$V_{in} > 50$ mV rms, See Figure 10
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		35	150	mV	Measured across Pins 2 and 3, $V_{in} = 0$, S_5 open
Voltage Comparator Section					
Open Loop Voltage Gain	66	80		dB	f = 20 Hz
Input Impedance	0.5	2		MΩ	Measured looking into Pin 1
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
Logic Output Section					Measured at Pin 8
Slew Rate		15		V/μsec	$R_L = 3$ kΩ, $C_L = 10$ pF, S_2 closed
"1" Output Leakage Current		0.02	10	μA	$V_0 = +24V$
"0" Output Voltage		0.2	0.4	V	$I_L = 10$ mA
Current Sink Capability	30	50		mA	$V_0 \leq 1V$

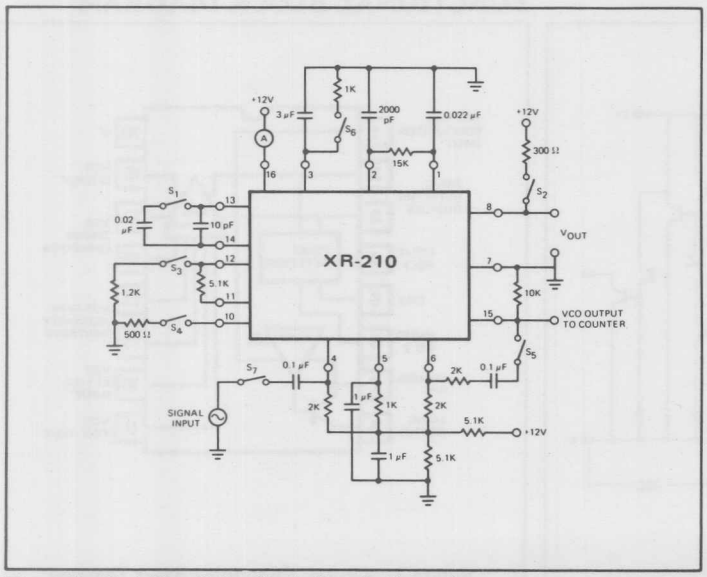


Figure 3. Test Circuit for Single Supply Operation

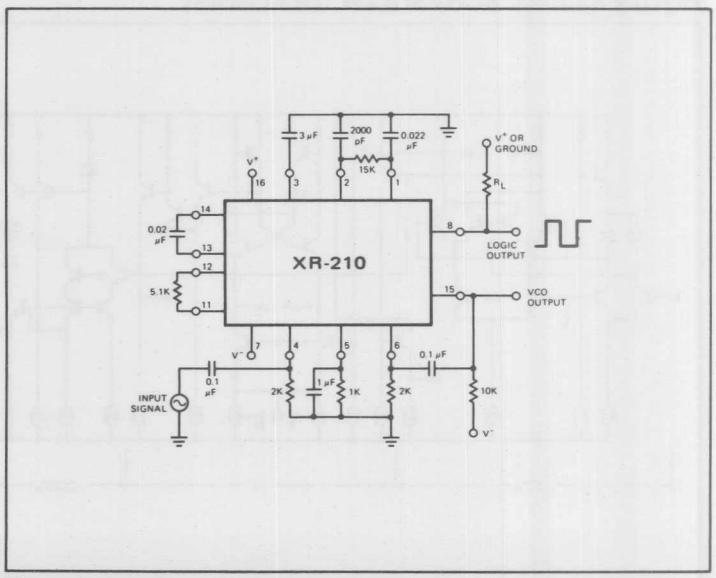


Figure 4. Test Circuit for Split Supply Operation

DESCRIPTION OF CIRCUIT CONTROLS

PHASE DETECTOR INPUTS (PINS 4 AND 6)

One input to the phase detector is used as the signal input; the remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see Figure 3). For split supply operation, these inputs are biased from ground as shown in Figure 4.

PHASE DETECTOR BIAS (PIN 5)

This terminal should be dc biased as shown in Figures 3 and 4 and ac grounded with a bypass capacitor. The bias resistor in series with this pin should be half as large as those in series with pins 4 and 6.

PHASE DETECTOR OUTPUTS (PINS 2 AND 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase-detector inputs (pins 4 and 6). These differential phase-detector outputs are internally connected to the VCO control terminals (see Figure 2). Pin 3 is also internally connected to the reference input of the voltage comparator section.

In normal use, the low-pass loop-filter capacitor, C1, is connected between pins 2 and 3. The 6K ohm impedances of the two outputs add for 12K ohms in the single-pole RC low-pass loop filter. Pin 2 is externally connected to the voltage comparator input (pin 1) through an RC low-pass filter.

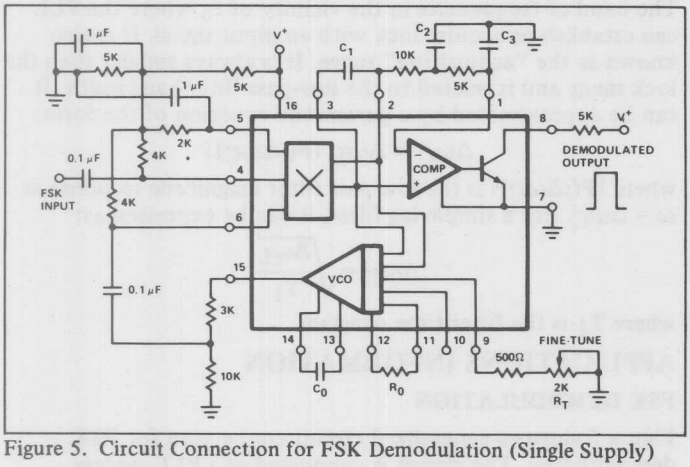


Figure 5. Circuit Connection for FSK Demodulation (Single Supply)

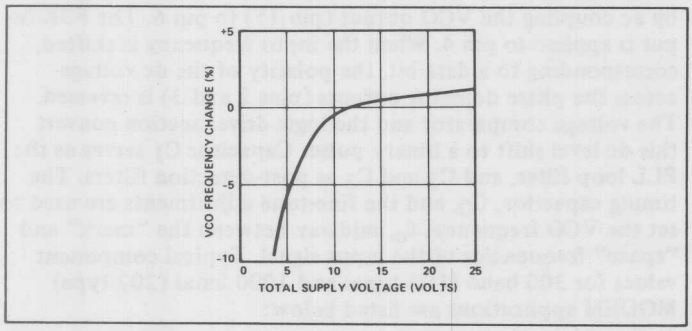


Figure 6. VCO Frequency Variation as a Function of Supply Voltage

VCO TIMING CAPACITOR (PINS 13 AND 14)

The VCO free-running frequency, f_o, is inversely proportional to timing capacitor, C_0 connected between pins 13 and 14. With pins 9 and 10 open-circuited, the VCO frequency is related to C_0 as:

$$f_o \approx \frac{220}{C_0} \text{ Hz}$$

where C_0 is in μF.

VCO OUTPUT (PIN 15)

The VCO produces approximately a 2.5 V_{p-p} squarewave output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 7 through a 10 kΩ resistor to increase the output current drive capability. For high voltage operation ($V_{CC} > 20V$), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output for short circuit protection.

VCO SWEEP INPUT (PIN 12)

The VCO frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see Figure 7). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 7. The VCO temperature dependence is minimum when the sweep input is not used. When the sweep input is not used, it should be left open circuited.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less under all operating conditions.

VCO CONVERSION GAIN (PIN 11)

The VCO voltage-to-frequency conversion gain, K_O, is inversely proportional to the value of external gain-control resistor, R_0, connected across pins 11 and 12.

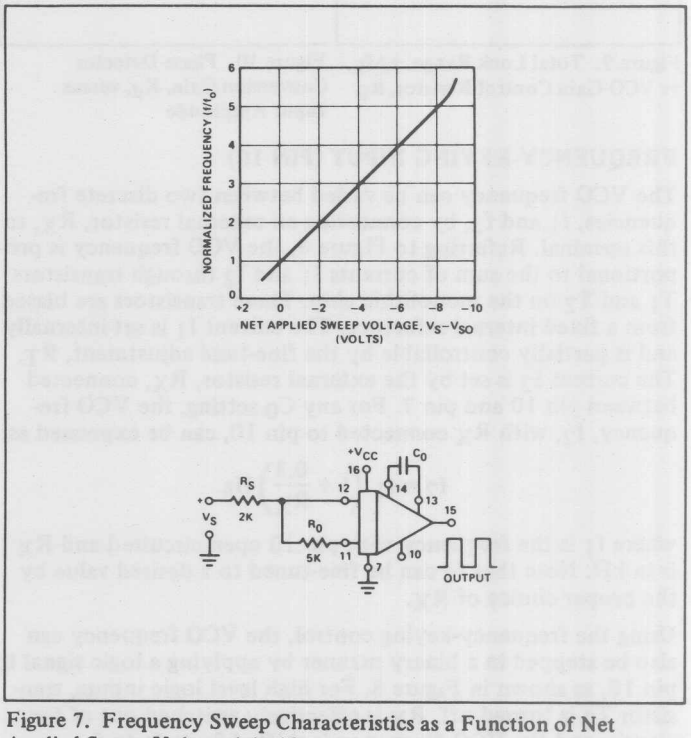


Figure 7. Frequency Sweep Characteristics as a Function of Net Applied Sweep Voltage (pin 10 open)

(Note: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

FINE TUNE CONTROL (PIN 9)

For a given choice of timing capacitor, C_0, the VCO frequency can be further fine-adjusted to a desired frequency, f_1, by means of a trimmer resistor, R_T, connected from pin 9 to pin 7, as shown in Figure 8. The fine tuned VCO frequency f_1 is related to R_T as:

$$f_1 \approx \frac{220}{C_0}\left(1 + \frac{0.1}{R_T}\right) \text{ Hz}$$

where C_0 is in μF and R_T is in kΩ.

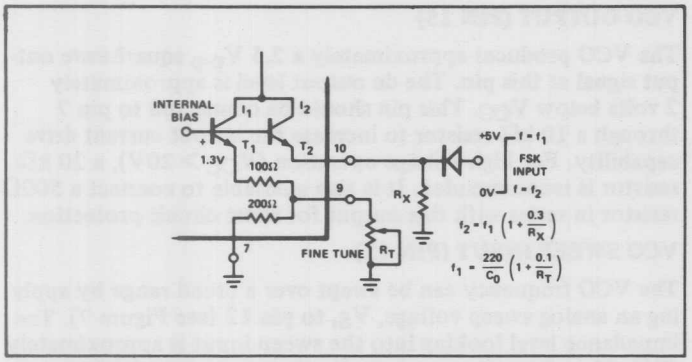


Figure 8. VCO Fine-Tune (Pin 9) and Frequency-Keying (Pin 10) Controls

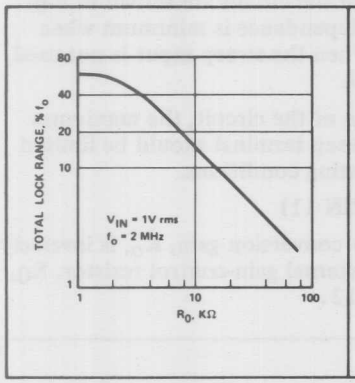


Figure 9. Total Lock Range, $\pm\Delta f_L$, vs VCO Gain Control Resistor, R_0

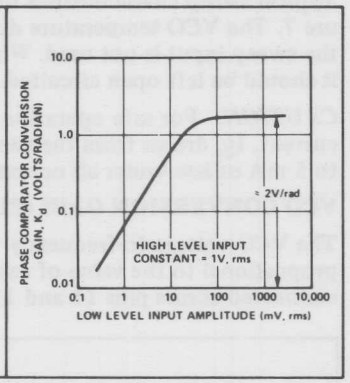


Figure 10. Phase Detector Conversion Gain, K_d, versus Input Amplitude

FREQUENCY-KEYING INPUT (PIN 10)

The VCO frequency can be varied between two discrete frequencies, f_1 and f_2, by connecting an external resistor, R_X, to this terminal. Referring to Figure 8, the VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I_1 is set internally and is partially controllable by the fine-tune adjustment, R_T. The current I_2 is set by the external resistor, R_X, connected between pin 10 and pin 7. For any C_0 setting, the VCO frequency, f_2, with R_X connected to pin 10, can be expressed as:

$$f_2 = f_1 \left(1 + \frac{0.3}{R_X}\right) \text{Hz}$$

where f_1 is the frequency with pin 10 open circuited and R_X is in kΩ. Note that f_2 can be fine-tuned to a desired value by the proper choice of R_X.

Using the frequency-keying control, the VCO frequency can also be stepped in a binary manner by applying a logic signal to pin 10, as shown in Figure 8. For high level logic inputs, transistor T_2 is turned off, R_X is effectively switched out of the circuit, and the VCO frequency is shifted from f_2 to f_1.

VOLTAGE COMPARATOR INPUT (PIN 1)

This pin provides the signal input to the voltage-comparator section. The comparator section is normally used for post-demodulation slicing and pulse-shaping. Normally, pin 1 is connected to pin 2 through a 15K external resistor, as shown in Figures 3 and 4. The input impedance level at this pin is approximately 2 MΩ.

LOGIC DRIVER OUTPUT (PIN 8)

This pin provides a binary logic output corresponding to the polarity of the input signal at the voltage comparator inputs. It is a "bare-collector" type stage with high current sinking capability.

DEFINITION OF TERMS

PHASE DETECTOR GAIN, K_d

K_d is the output voltage from the phase detector per radian of phase difference at the phase detector inputs (pins 4 and 6). K_d is proportional to the input signal for low level inputs ($\leq$ 25 mV rms) and is constant at high input levels (see Figure 10).

VCO CONVERSION GAIN, K_0

$$K_o \approx \frac{700}{C_0 R_0} \quad \text{(radians/sec)/volt}$$

where C_0 is in μF and R_0 is in kΩ. For most applications, recommended values for R_0 range from 1 kΩ to 10 kΩ.

When the XR-210 is connected as a PLL, its lock range can be controlled by varying the VCO gain control resistor, R_0, across pins 11 and 12. For input signals greater than 30 mV rms, the PLL loop gain is independent of signal amplitude but is inversely proportional to R_0. Figure 9 shows the dependence of lock range, $\pm\Delta f_L$, on R_0.

LOCK RANGE ($\Delta\omega_L$)

The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. If saturation or limiting does not occur, the lock range is equal to the loop gain, i.e. $\Delta\omega_L = K_T = K_d K_o$.

CAPTURE RANGE ($\Delta\omega_C$)

The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L \, |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C)|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

where T_1 is the filter time constant.

APPLICATIONS INFORMATION

FSK DEMODULATION

Figure 5 shows a generalized circuit connection for FSK demodulation. The circuit is connected as a PLL system by ac coupling the VCO output (pin 15) to pin 6. The FSK input is applied to pin 4. When the input frequency is shifted, corresponding to a data bit, the polarity of the dc voltage across the phase detector outputs (pins 2 and 3) is reversed. The voltage comparator and the logic driver section convert this dc level shift to a binary pulse. Capacitor C_1 serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. The timing capacitor, C_0, and the fine-tune adjustments are used to set the VCO frequency, f_o, midway between the "mark" and "space" frequencies of the input signal. Typical component values for 300 baud (103-type) and 1200 baud (202-type) MODEM applications are listed below:

OPERATING CONDITIONS		TYPICAL COMPONENT VALUES
300 Baud		
Low Band:	f_1 = 1070 Hz	R_0 = 5.1 KΩ, C_0 = 0.22 μF
	f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF, C_3 = 0.033 μF
High Band:	f_1 = 2025 Hz	R_0 = 8.2 KΩ, C_0 = 0.1 μF
	f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1200 Baud		R_0 = 2 KΩ, C_0 = 0.14 μF
	f_1 = 1200 Hz	C_1 = 0.033 μF, C_3 = 0.02 μF
	f_2 = 2200 Hz	C_2 = 0.01 μF

XR-215

Monolithic Phase-Locked Loop

OCTOBER 1973

The XR-215 is a highly versatile monolithic phase-locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on-off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single external capacitor. The operational amplifier can be used for audio preamplification in FM detector applications; or, as a high speed sense amplifier (or comparator) in FSK demodulation.

FEATURES

Wide Frequency Range: 0.5 Hz to 35 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL and ECL Logic Compatibility
Wide Dynamic Range: 300 μV to 3V
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to ±50%
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65dB

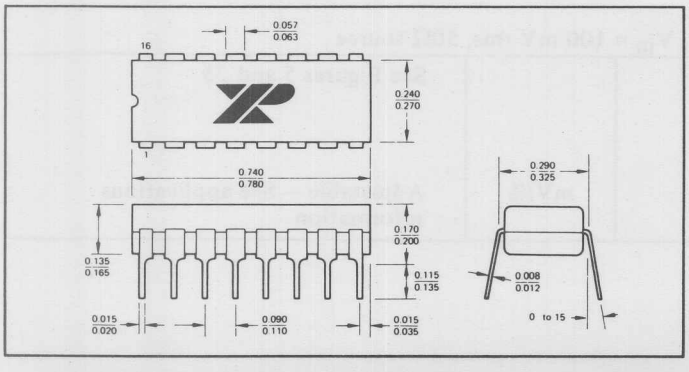
APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
Tone Decoding
Data Synchronization
Telemetry Coding/Decoding
FM, FSK and Sweep Generation
Crystal Controlled Detection
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation	750 mW
Derate above +25°C	5 mW/°C
Temperature	
Operating	−55°C to +125°C
Storage	−65°C to +150°C

PACKAGE INFORMATION (ceramic)



FUNCTIONAL BLOCK DIAGRAM

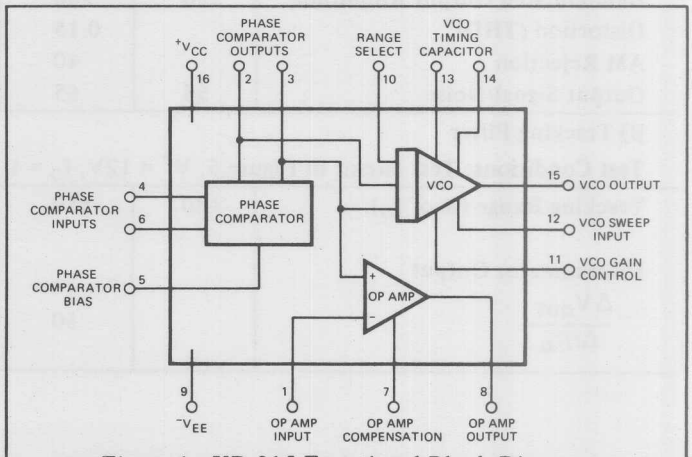


Figure 1. XR-215 Functional Block Diagram

ELECTRICAL SPECIFICATIONS

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
I – General Characteristics **Test Conditions:** V^+ = 12V (single supply), T_A = 25°C, Test Circuit of Figure 2 with C_0 = 100 pF, (silver-mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.					
Supply Voltage:					
Single Supply	5		26	V dc	See Figure 2
Split Supply	±2.5		±13	V dc	See Figure 3
Supply Current	8	11	15	mA	See Figure 2
Upper Frequency Limit	20	35		MHz	See Figure 2, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500 μF
VCO Section:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 2, 0°C ≤ T_A ≤ 75°C
Power Supply		0.1		%/V	$V^+ > 10V$
Sweep Range	5:1	8:1			S_3 closed, S_4 open, $0 < V_S < 6V$ See Figure 9, C_0 = 2000 pF
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Rise Time		20		ns	10 pF to ground at Pin 15
Fall Time		20		ns	
Phase Comparator Section:					
Conversion Gain		2		V/rad	$V_{in} > 50$ mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	100	mV	Measured across Pins 2 and 3 V_{in} = 0, S_5 open
Op Amp Section:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/μ sec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		V_{p-p}	R_L = 30 kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
II – Special Applications A) FM Demodulation: **Test Conditions:** Test circuit of Figure 4, V^+ = 12V, input signal = 10.7 MHz FM with Δf = 75 kHz, f_{mod} = 1 kHz					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude	250	500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{in} = 10 mV rms, 30% AM
Output Signal/Noise	55	65		dB	
B) Tracking Filter **Test Conditions:** Test circuit of Figure 5, V^+ = 12V, f_o = 1 MHz, V_{in} = 100 mV rms, 50Ω source					
Tracking Range (% of f_o)	±30	±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{out}}{\Delta f/f_o}$		50		mV/%	Adjustable – See applications information

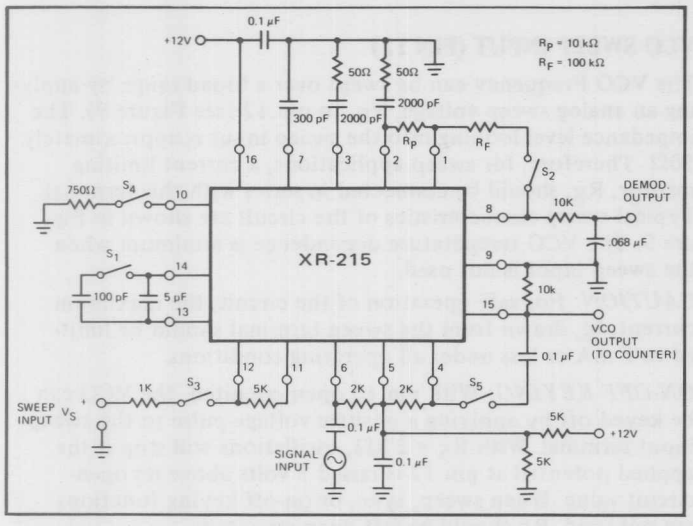


Figure 2. Test Circuit For Single Supply Operation

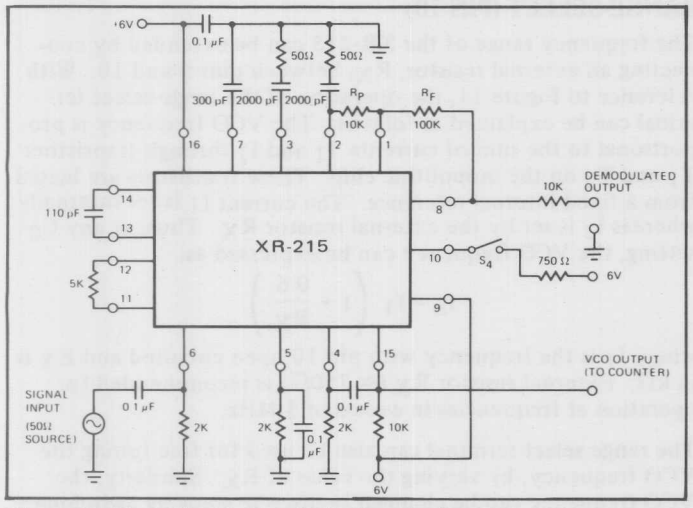


Figure 3. Test Circuit For Split-Supply Operation

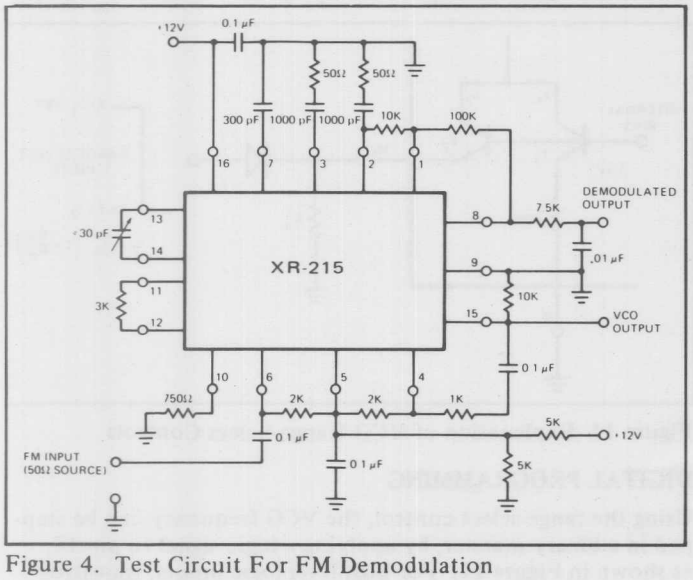


Figure 4. Test Circuit For FM Demodulation

DESCRIPTION OF CIRCUIT CONTROLS

PHASE COMPARATOR INPUTS (PINS 4 AND 6)

One input to the phase comparator is used as the signal input; the remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see Figure 2). For split supply operation, these inputs are biased from ground as shown in Figure 3. For single supply operation, a resistive bias string similar to that shown in Figure 2 should be used to set the bias level at approximately $V_{CC}/2$. The dc bias current at these terminals is nominally 8 μA.

PHASE COMPARATOR BIAS (PIN 5)

This terminal should be dc biased as shown in Figures 2 and 3, and ac grounded with a bypass capacitor.

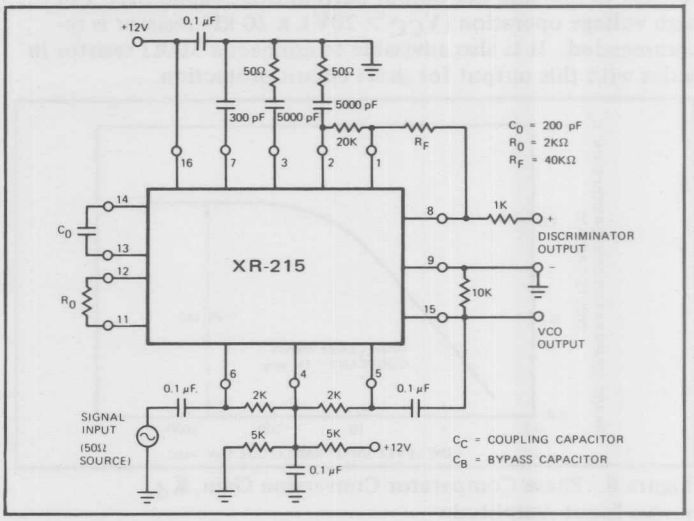


Figure 5. Test Circuit For Tracking Filter

PHASE COMPARATOR OUTPUTS (PINS 2 AND 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase comparator inputs (pins 4 and 6). The phase comparator outputs are internally connected to the VCO control terminals (see Figure 1). One of the outputs (pin 3) is internally connected to the *non-inverting* input of the operational amplifier. The low-pass filter is achieved by connecting an RC network to the phase comparator outputs as shown in Figure 14.

VCO TIMING CAPACITOR (PINS 13 AND 14)

The VCO free-running frequency, f_O, is inversely proportional to timing capacitor C_0 connected between pins 13 and 14. (See Figure 7).

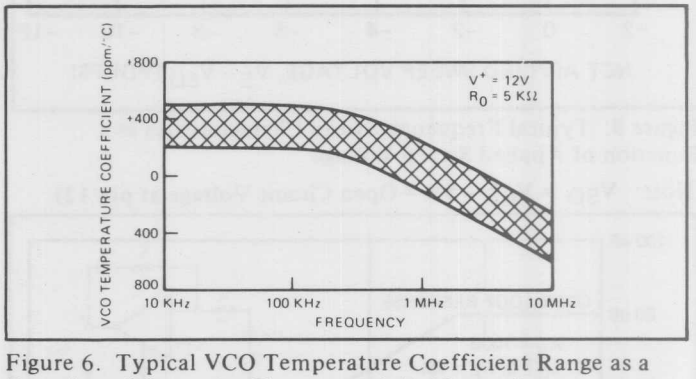


Figure 6. Typical VCO Temperature Coefficient Range as a Function of Operating Frequency (pin 10 open)

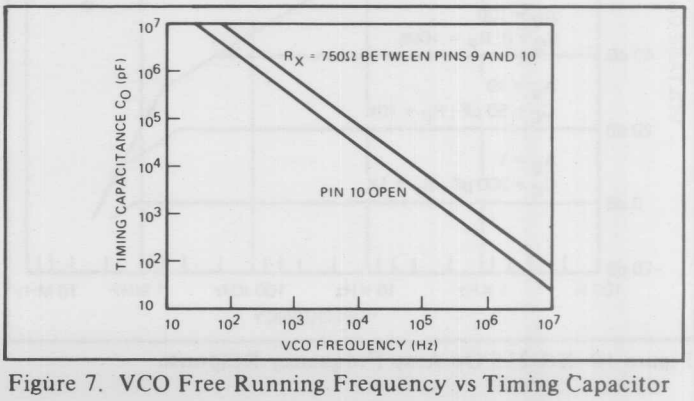


Figure 7. VCO Free Running Frequency vs Timing Capacitor

VCO OUTPUT (PIN 15)

The VCO produces approximately a 2.5 V_{p-p} output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 9 through a 10 kΩ resistor to increase the output current drive capability. For high voltage operation ($V_{CC} > 20V$), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output for short circuit protection.

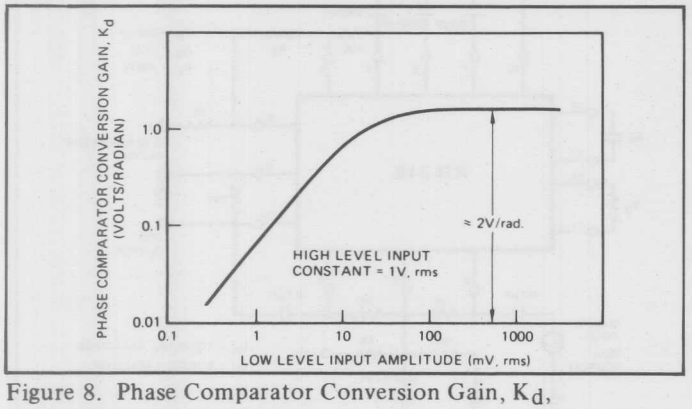


Figure 8. Phase Comparator Conversion Gain, K_d, versus Input Amplitude

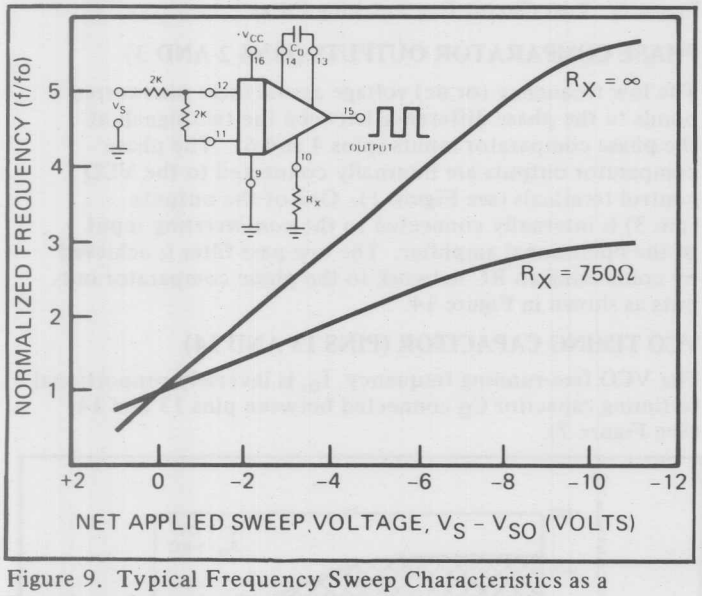


Figure 9. Typical Frequency Sweep Characteristics as a Function of Applied Sweep Voltage

(Note: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

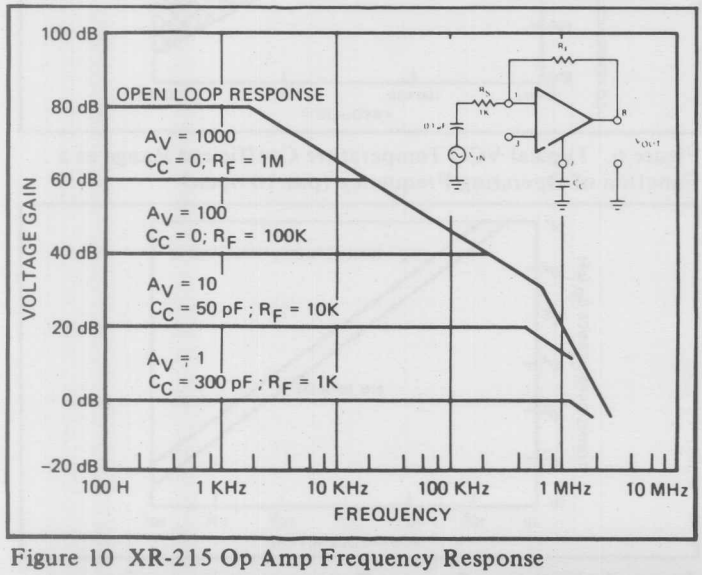


Figure 10 XR-215 Op Amp Frequency Response

VCO SWEEP INPUT (PIN 12)

The VCO Frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see Figure 9). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 9. The VCO temperature dependence is minimum when the sweep input is not used.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less under all operating conditions.

ON-OFF KEYING: With pin 10 open circuited, the VCO can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 2 kΩ, oscillations will stop if the applied potential at pin 12 is raised 3 volts above its open-circuit value. When sweep, sync, or on-off keying functions are not used, R_S should be left open circuited.

RANGE-SELECT (PIN 10)

The frequency range of the XR-215 can be extended by connecting an external resistor, R_X, between pins 9 and 10. With reference to Figure 11, the operation of the range-select terminal can be explained as follows: The VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I_1 is set internally, whereas I_2 is set by the external resistor R_X. Thus, at any C_0 setting, the VCO frequency can be expressed as:

$$f_o = f_1 \left(1 + \frac{0.6}{R_X}\right)$$

where f_1 is the frequency with pin 10 open circuited and R_X is in kΩ. External resistor R_X (≈ 750Ω) is recommended for operation at frequencies in excess of 5 MHz.

The range select terminal can also be used for fine tuning the VCO frequency, by varying the value of R_X. Similarly, the VCO frequency can be changed in discrete steps by switching in different values of R_X between pins 9 and 10.

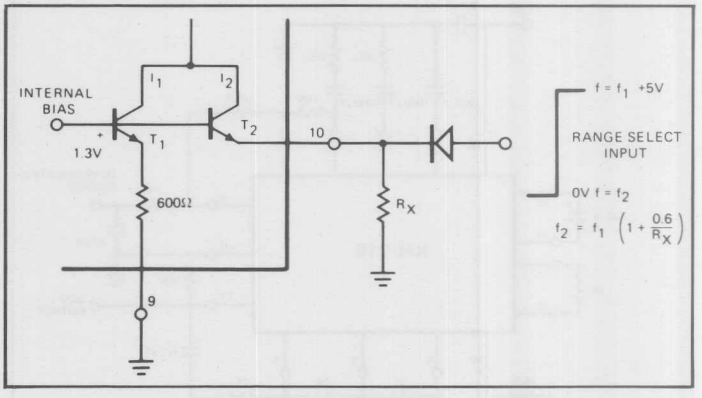


Figure 11 Explanation of VCO Range-Select Controls

DIGITAL PROGRAMMING

Using the range select control, the VCO frequency can be stepped in a binary manner, by applying a logic signal to pin 10, as shown in Figure 11. For high level logic inputs, transistor T_2 is turned off, and R_X is effectively switched out of the circuit. Using the digital programming capability, the XR-215 can be time-multiplexed between two separate input frequencies, as shown in Figures 18 and 19.

AMPLIFIER INPUT (PIN 1)

This pin provides the inverting input for the operational amplifier section. Normally it is connected to pin 2 through a 10 kΩ external resistor (see Figure 2 or 3).

AMPLIFIER OUTPUT (PIN 8)

This pin is used as the output terminal for FM or FSK demodulation. The amplifier gain is determined by the external feedback resistor, R_F, connected between pins 1 and 8. Frequency response characteristics of the amplifier section are shown in Figure 10.

AMPLIFIER COMPENSATION (PIN 7)

The operational amplifier can be compensated by a single 300 pF capacitor from pin 7 to ground. (See Figure 10).

BASIC PHASE-LOCKED LOOP OPERATION

PRINCIPLE OF OPERATION

The phase-locked loop (PLL) is a unique and versatile circuit technique which provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 12, the PLL is a feedback system comprised of three basic functional blocks: phase comparator, low-pass filter and voltage-controlled oscillator (VCO). The basic principle of operation of a PLL can be briefly explained as follows: with no input signal applied to the system, the error voltage V_d, is equal to zero. The VCO operates at a set frequency, f_o, which is known as the "free-running" frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

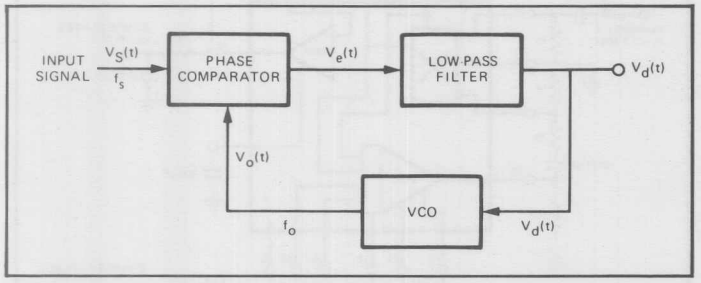


Figure 12 Block Diagram of a Phase-Locked Loop

A LINEARIZED MODEL FOR PLL

When the PLL is in lock, it can be approximated by the linear feedback system shown in Figure 13. ϕ_S and ϕ_O are the respective phase angles associated with the input signal and the VCO output, F(s) is the low-pass filter response in frequency domain, and K_d and K_O are the conversion gains associated with the phase comparator and VCO sections of the PLL.

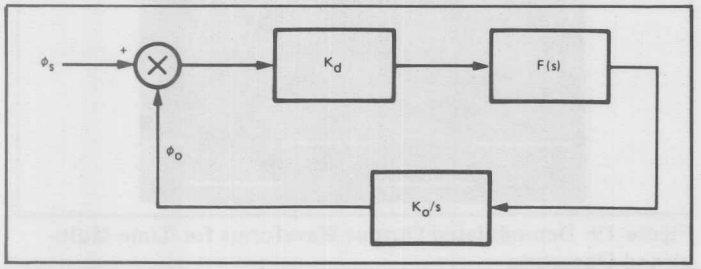


Figure 13 Linearized Model of a PLL as a Negative Feedback system

DEFINITION OF XR-215 PARAMETERS FOR PLL APPLICATIONS

VCO FREE-RUNNING FREQUENCY, f_o

The VCO frequency with no input signal. It is determined by selection of C_0 across pins 13 and 14 and can be increased by connecting an external resistor R_X between pins 9 and 10. It can be approximated as:

$$f_o = \frac{200}{C_0}\left(1 + \frac{0.6}{R_X}\right)$$

where C_0 is in μF and R_X is in kΩ. (See Figure 7).

PHASE COMPARATOR GAIN K_d

The output voltage from the phase comparator per radian of phase difference at the phase comparator inputs (pins 4 and 6).

VCO CONVERSION GAIN K_o

The VCO voltage-to-frequency conversion gain is determined by the choice of timing capacitor C_0 and gain control resistor, R_0 connected externally across pins 11 and 12. It can be expressed as

$$K_o \approx \frac{700}{C_0 R_0} \text{ (radians/sec)/volt}$$

where C_0 is in μF and R_0 is in kΩ. For most applications, recommended values for R_0 range from 1 kΩ to 10 kΩ.

LOCK RANGE ($\Delta\omega_L$)

The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the "tracking" or "holding" range. If saturation or limiting does not occur, the lock range is equal to the loop gain, i.e. $\Delta\omega_L = K_T = K_d K_o$.

CAPTURE RANGE ($\Delta\omega_C$)

The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

where T_1 is the filter time constant.

AMPLIFIER GAIN A_V

The voltage gain of the amplifier section is determined by feedback resistors R_F and R_P between pins (8,1) and (2,1) respectively. (See Figures 2 and 3). It is given by:

$$A_V = \frac{-R_F}{R_1 + R_P}$$

where R_1 is the 6 kΩ internal impedance at pin 2, and R_p is the external resistor between pins 1 and 2.

LOW-PASS FILTER

The low-pass filter section is formed by connecting an external capacitor or RC network across terminals 2 and 3. The low-pass filter components can be connected either between pins 2 and 3 or, from each pin to ground. Typical filter configurations and corresponding filter transfer functions are shown in Figure 14 where R_1 (6 kΩ) is the internal impedance at pins 2 and 3.

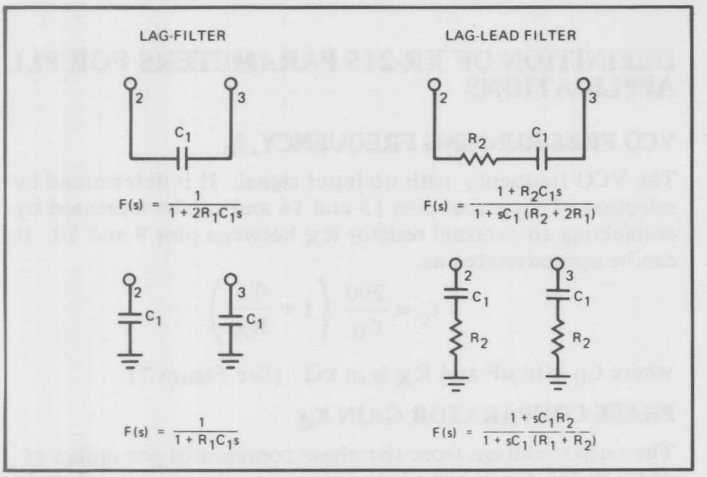


Figure 14

APPLICATIONS INFORMATION

FM DEMODULATION

Figure 15 shows the external circuit connections to the XR-215 for frequency-selective FM demodulation. The choice of C_0 is determined by the FM carrier frequency (see Figure 7). The low-pass filter capacitor C_1 is determined by the selectivity requirements. For carrier frequencies of 1 to 10 MHz, C_1 is in the range of 10 C_0 to 30 C_0. The feedback resistor R_F can be used as a "volume-control" adjustment to set the amplitude of the demodulated output. The demodulated output amplitude is proportional to the FM deviation and to resistors R_0 and R_F. For ±1% FM deviation it can be approximated as:

$$V_{OUT} \approx R_0 R_F \left(1 + \frac{0.6}{R_X}\right) \text{ mV, rms}$$

where all resistors are in kΩ and R_X is the range extension resistor connected across pins 9 and 10. For circuit operation below 5 MHz, R_X can be open circuited. For operation above 5 MHz, $R_X \approx 750\Omega$ is recommended.

Typical output signal/noise ratio and harmonic distortion are shown in Figures 16 and 17 as a function of FM deviation, for the component values shown in Figure 4.

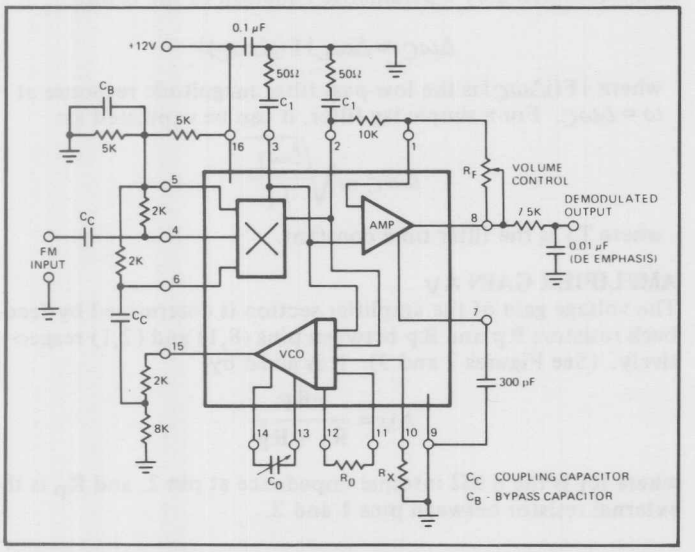


Figure 15 Circuit Connection for FM Demodulation

MULTI-CHANNEL DEMODULATION

The ac digital programming capability of the XR-215 allows a single circuit be time-shared or multiplexed between two information channels, and thereby selectively demodulate two separate carrier frequencies. Figure 18 shows a practical circuit configuration for time-multiplexing the XR-215 between two FM channels, at 1 MHz and 1.1 MHz respectively. The channel-select logic signal is applied to pin 10, as shown in Figure 18, with both input channels simultaneously present at the PLL input (pin 4). Figure 19 shows the demodulated output as a function of the channel-select pulse where the two inputs have sinusoidal and triangular FM modulation respectively.

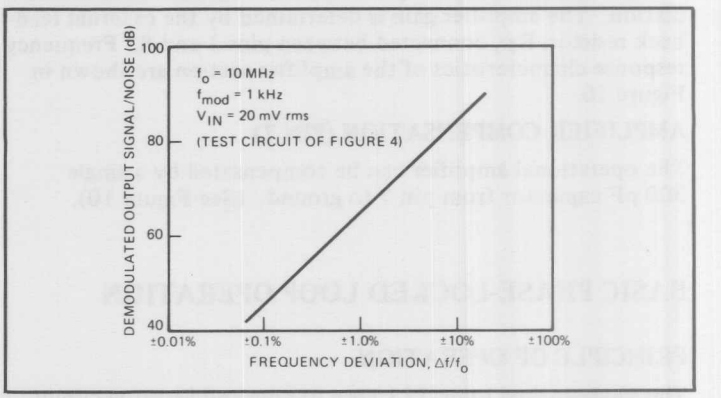


Figure 16 Output Signal/Noise Ratio as a Function of FM Deviation

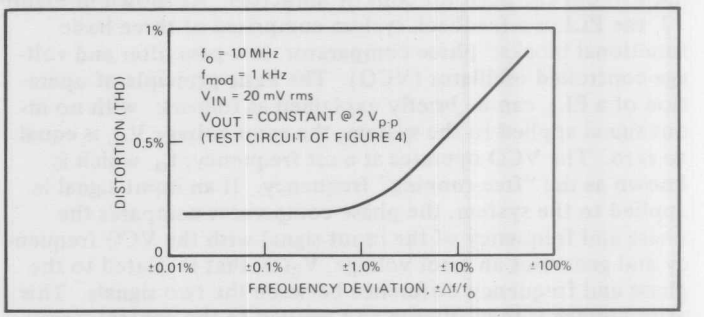


Figure 17 Output Distortion as a Function of FM Deviation

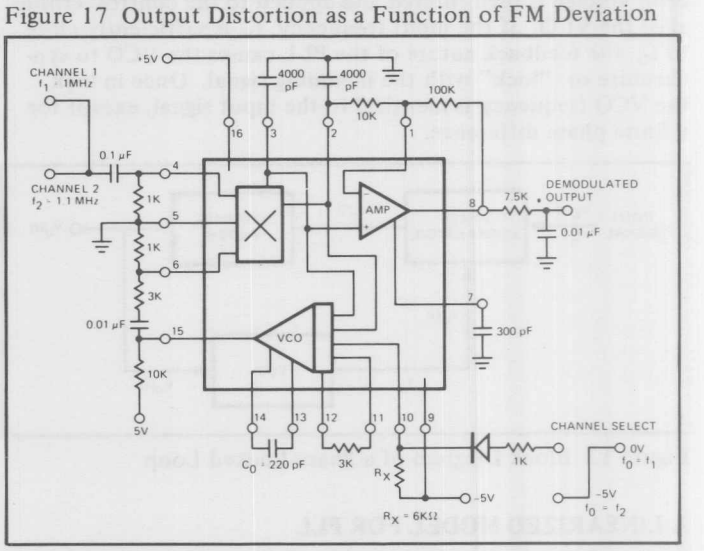


Figure 18 Time-Multiplexing XR-215 Between Two Simultaneous FM Channels

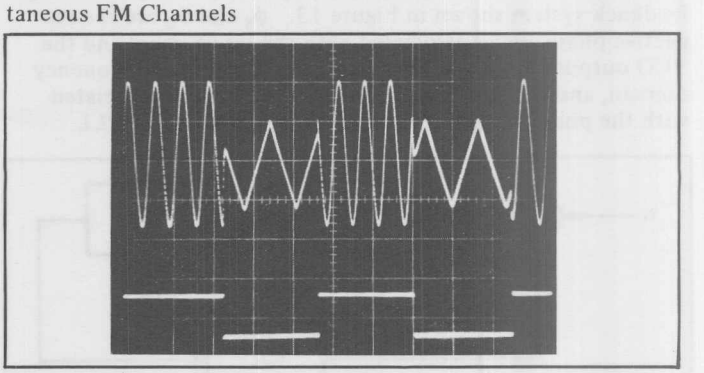


Figure 19 Demodulated Output Waveforms for Time-Multiplexed Operation

Top: Demodulated Output
Sinewave - Channel 1
Triangle Wave - Channel 2

Bottom: Channel Select Pulse

FSK DEMODULATION

Figure 20 contains a typical circuit connection for FSK demodulation. When the input frequency is shifted, corresponding to a data bit, the dc voltage at the phase comparator outputs (pins 2 and 3) also reverses polarity. The operational amplifier section is connected as a comparator, and converts the dc level shift to a binary output pulse. One of the phase

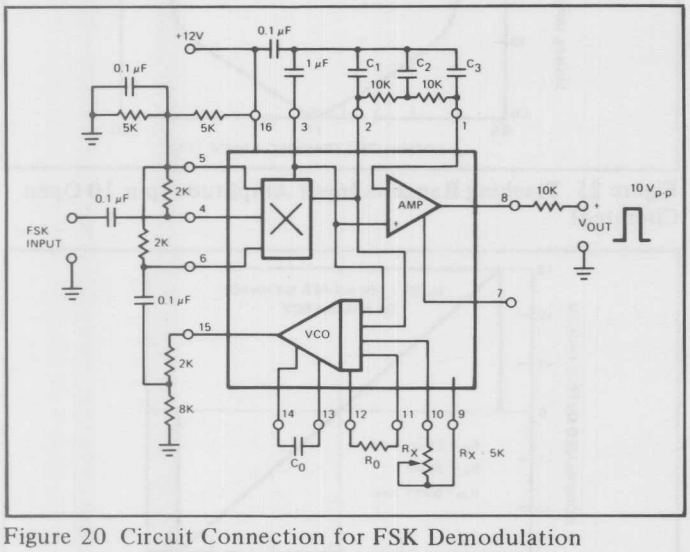


Figure 20 Circuit Connection for FSK Demodulation

comparator outputs (pin 3) is ac grounded and serves as the bias reference for the operational amplifier section. Capacitor C_1 serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. Range select resistor, R_X, can be used as a fine-tune adjustment to set the VCO frequency.

Typical component values for 300 baud and 1800 baud operation are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070 Hz	R_0 = 5 kΩ, C_0 = 0.17 μF
f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF, C_3 = 0.033 μF
High Band: f_1 = 2025 Hz	R_0 = 8 kΩ, C_0 = 0.1 μF
f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1800 Baud	R_0 = 2 kΩ, C_0 = 0.12 μF
f_1 = 1200 Hz	$C_1 = C_3$ = 0.003 μF,
f_2 = 2200 Hz	C_2 = 0.01 μF

Note that for 300 Baud operation the circuit can be time-multiplexed between high and low bands by switching the external resistor R_X in and out of the circuit with a control signal, as shown in Figure 11.

FSK GENERATION

The digital programming capability of the XR-215 can be used for FSK generation. A typical circuit connection for this application is shown in Figure 21. The VCO frequency can be shifted between the mark (f_2) and space (f_1) frequencies by applying a logic pulse to pin 10. The circuit can provide two separate FSK outputs: a low level (2.5 V_{p-p}) output at pin 15 or a high amplitude (10 V_{p-p}) output at pin 8. The output at each of these terminals is a symmetrical squarewave with a typical second harmonic content of less than 0.3%.

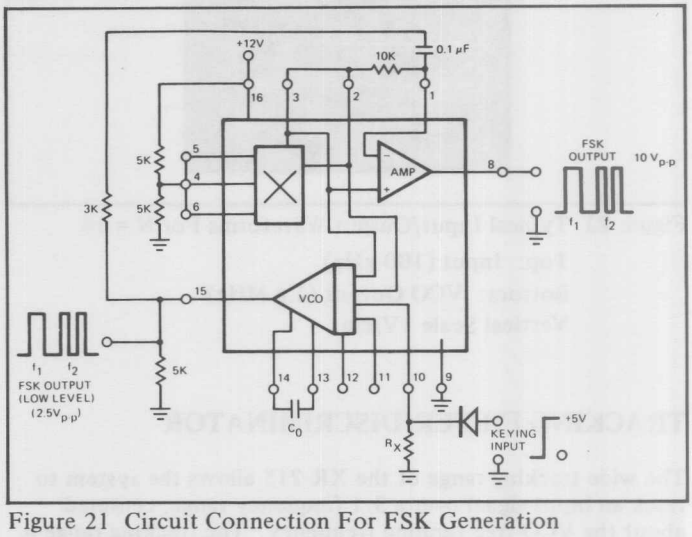


Figure 21 Circuit Connection For FSK Generation

FREQUENCY SYNTHESIS

In frequency synthesis applications, a programmable counter or divide-by-N circuit is connected between the VCO output (pin 15) and one of the phase detector inputs (pins 4 or 6), as shown in Figure 22. The principle of operation of the circuit can be briefly explained as follows: The counter divides down the oscillator frequency by the programmable divider modulus, N. Thus, when the entire system is phase-locked to an input signal at frequency, f_s, the oscillator output at pin 15 is at a frequency (Nf_s), where N is the divider modulus. By proper choice of the divider modulus, a large number of discrete frequencies can be synthesized from a given reference frequency. The low-pass filter capacitor C_1 is normally chosen to provide a cut-off frequency equal to 0.1% to 2% of the signal frequency, f_s.

The circuit was designed to operate with commercially available monolithic programmable counter circuits using TTL logic, such as MC4016, SN5493 or equivalent. The digital or analog tuning characteristics of the VCO can be used to extend the available range of frequencies of the system, for a given setting of the timing capacitor C_0.

Typical input and output waveforms for N = 16 operation with with f_s = 100 kHz and f_o = 1.6 MHz are shown in Figure 23.

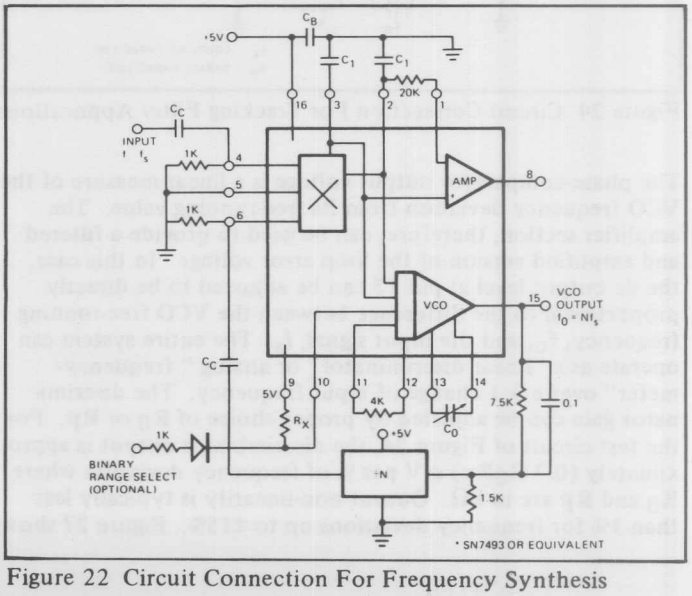


Figure 22 Circuit Connection For Frequency Synthesis

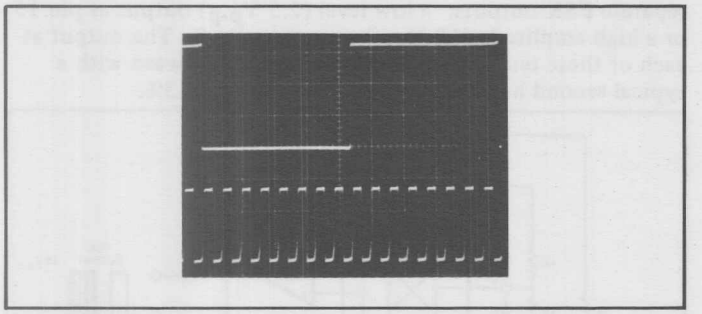


Figure 23 Typical Input/Output Waveforms For N = 16
Top: Input (100 kHz)
Bottom: VCO Output (1.6 MHz)
Vertical Scale 1V/cm

TRACKING FILTER/DISCRIMINATOR

The wide tracking range of the XR-215 allows the system to track an input signal over a 3:1 frequency range, centered about the VCO free running frequency. The tracking range is maximum when the binary range-select (pin 10) is open circuited. The circuit connections for this application are shown in Figure 24. Typical tracking range for a given input signal amplitude is shown in Figure 25. Recommended values of external components are: 1 kΩ < R_0 < 4 kΩ and 30 C_0 < C_1 < 300 C_0 where the timing capacitor C_0 is determined by the center frequency requirements (see Figure 7).

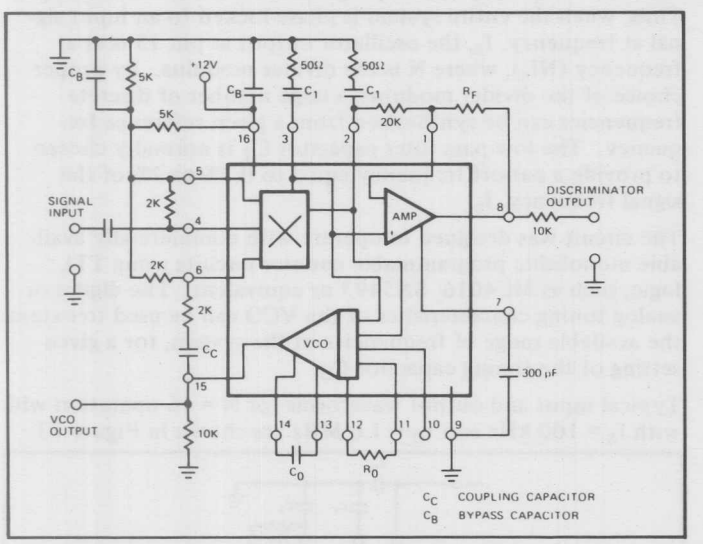


Figure 24 Circuit Connection For Tracking Filter Applications

The phase-comparator output voltage is a linear measure of the VCO frequency deviation from its free-running value. The amplifier section, therefore, can be used to provide a filtered and amplified version of the loop error voltage. In this case, the dc output level at pin 15 can be adjusted to be directly proportional to the difference between the VCO free-running frequency, f_o, and the input signal, f_s. The entire system can operate as a "linear discriminator" or analog " frequency-meter" over a 3:1 change of input frequency. The discriminator gain can be adjusted by proper choice of R_0 or R_F. For the test circuit of Figure 24, the discriminator output is approximately (0.7 R_0R_F) mV per % of frequency deviation where R_0 and R_F are in kΩ. Output non-linearity is typically less than 1% for frequency deviations up to ±15%. Figure 27 shows the normalized output characteristics as a function of input frequency, with R_0 = 2 kΩ and R_F = 36 kΩ.

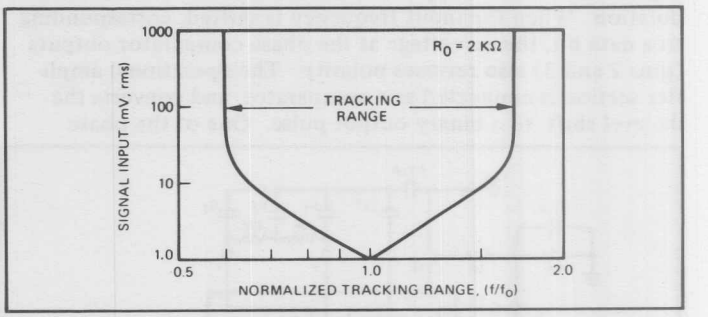


Figure 25 Tracking Range vs Input Amplitude (pin 10 Open Circuited)

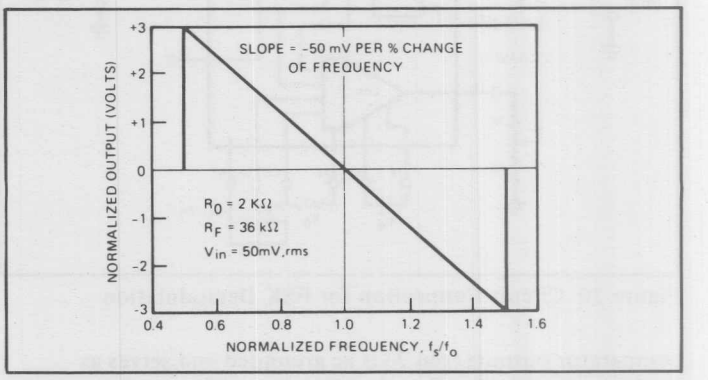


Figure 26. Typical Discriminator Output Characteristics For Tracking Filter Applications

CRYSTAL-CONTROLLED PLL

The XR-215 can be operated as a crystal-controlled phase-locked loop by replacing the timing capacitor with a crystal. A circuit connection for this application is shown in Figure 26. Normally a small tuning capacitor (≈ 30 pF) is required in series with the crystal to set the crystal frequency. For this application the crystal should be operated in its fundamental mode. Typical pull-in range of the circuit is ±1 kHz at 10 MHz.

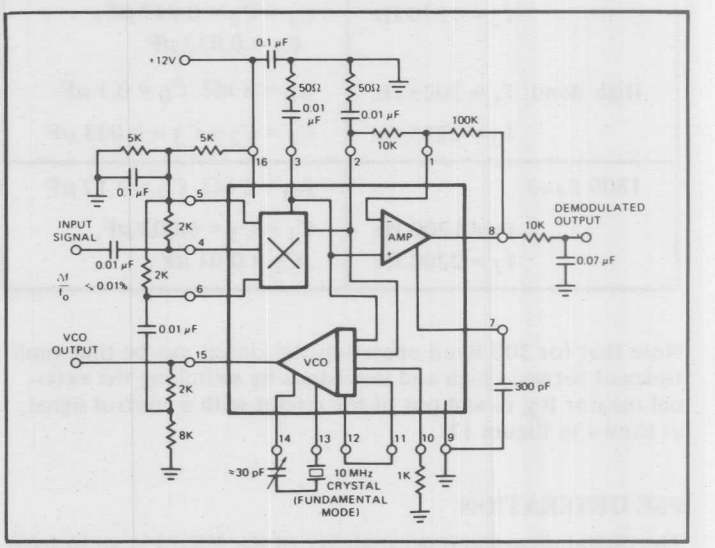


Figure 27 Typical Circuit Connection For Crystal-Controlled FM Detection

XR-2211

FSK Demodulator/Tone Decoder

OCTOBER 1976

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier-Detection	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

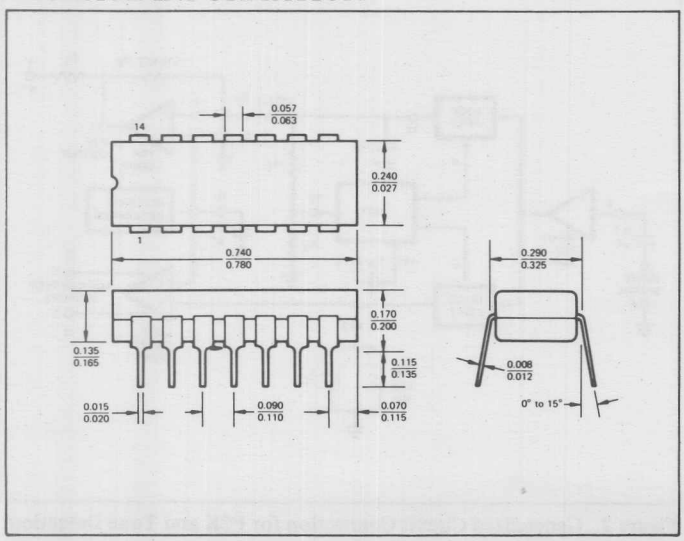
ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mV/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5.0 mW/°C

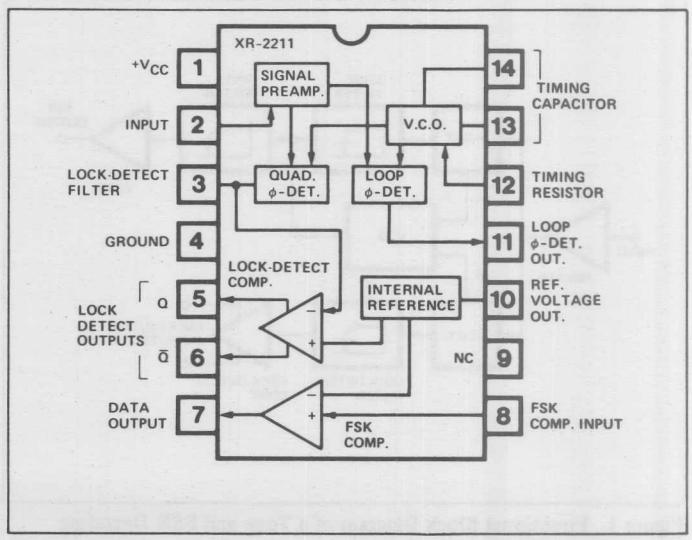
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	-55°C to +125°C
XR-2211CN	Ceramic	0°C to +75°C
XR-2211CP	Plastic	0°C to +75°C
XR-2211N	Ceramic	-40°C to +85°C
XR-2211P	Plastic	-40°C to +85°C

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30\ K\Omega$, $C_0 = 0.033\ \mu F$. See Fig. 2 for component designation

CHARACTERISTICS	XR-2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Current		4	7		5	9	mA	$R_0 \geq 10\ K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$. See Fig. 7.
		0.2			0.2		%/V	$V^+ = 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ K\Omega$, $C_0 = 400\ pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		μA	
Output Impedance		1			1		MΩ	
Maximum Swing		11			11		Vpp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		KΩ	
Input Signal								
Voltage Required to Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTIONS								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ K\Omega$
Output Voltage Low		300			300		mV	$I_C = 3\ mA$
Output Leakage Current		.01			.01		μA	$V_O = 12V$
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	

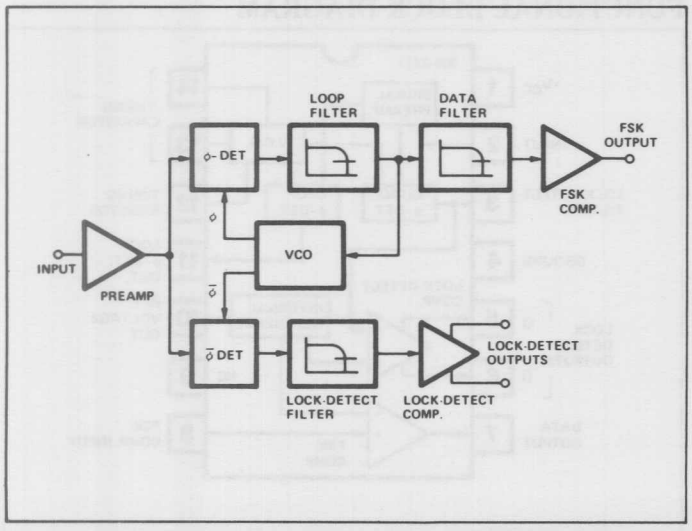


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

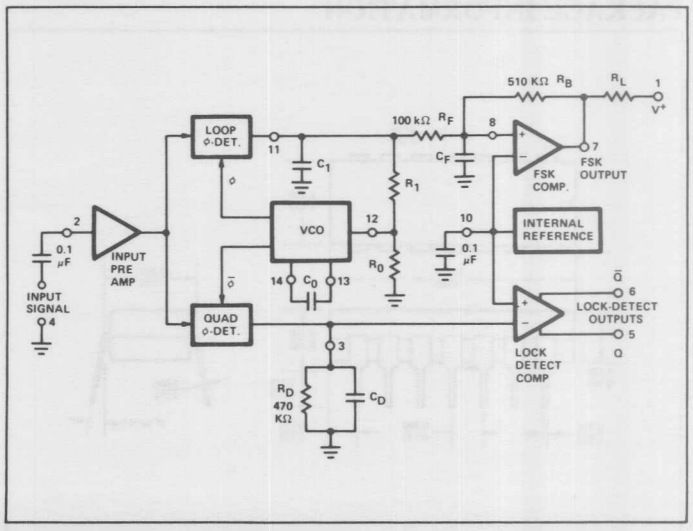


Figure 2. Generalized Circuit Connection for FSK and Tone Detection.

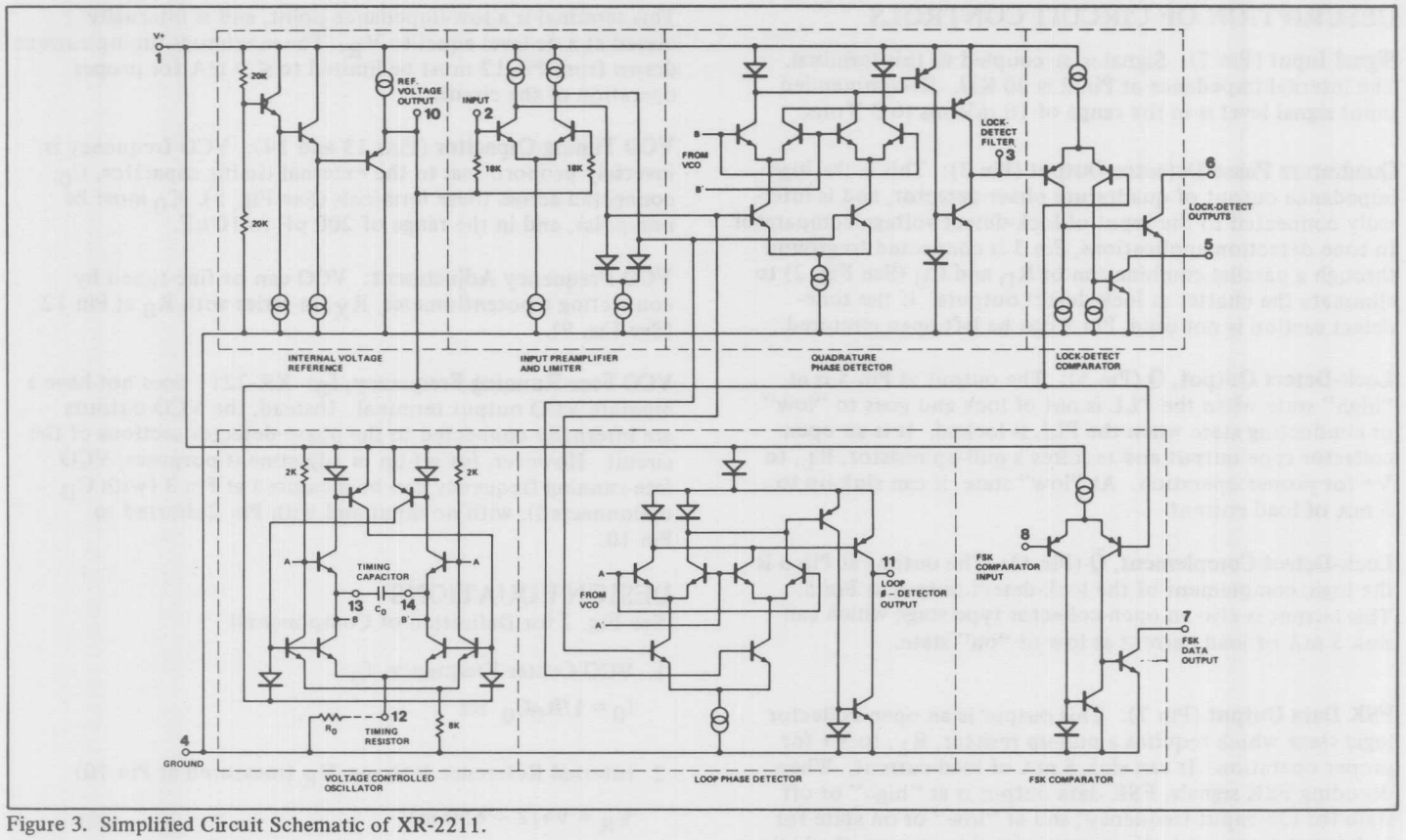


Figure 3. Simplified Circuit Schematic of XR-2211.

TYPICAL CHARACTERISTICS

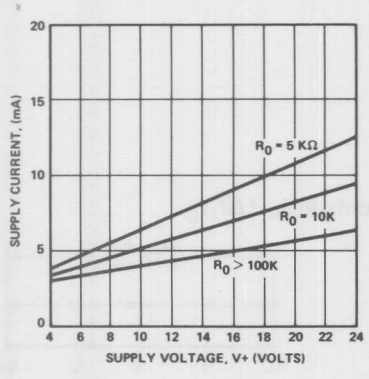


Figure 4. Typical Supply Current vs V^+ (Logic Outputs Open Circuited).

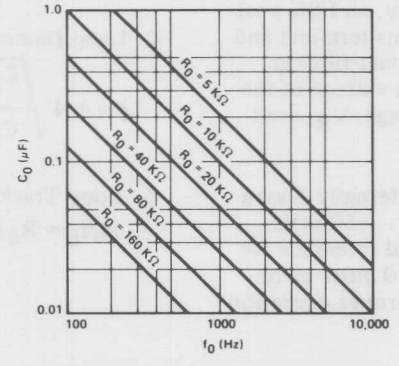


Figure 5. VCO Frequency vs Timing Resistor

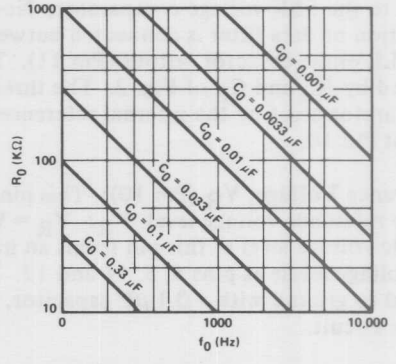


Figure 6. VCO Frequency vs Timing Capacitor

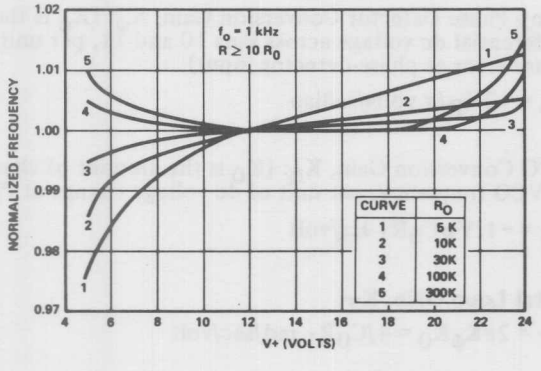


Figure 7. Typical f_0 vs Power Supply Characteristics.

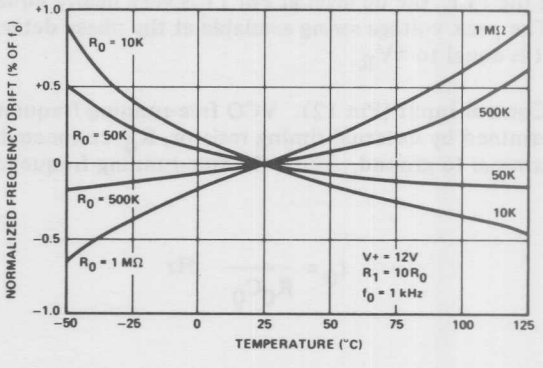


Figure 8. Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mVrms to 3 Vrms.

Quadrature Phase Detector Output (Pin 3): This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (See Fig. 2) to eliminate the chatter at lock-detect outputs. If the tone-detect section is not used, Pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

Lock-Detect Complement, $\overline{Q}$ (Pin 6): The output at Pin 6 is the logic complement of the lock-detect output at Pin 5. This output is also an open-collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open-collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency; and at "low" or on state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (Pin 11). This data filter is formed by R_F and C_F of Fig. 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 *must* be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (See Fig. 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \quad \text{Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ (See Fig. 8).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤ 3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (See Fig. 5). C_0 must be non-polar, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (See Fig. 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with C_D disconnected), with no input and with Pin 2 shorted to Pin 10.

DESIGN EQUATIONS

(See Fig. 2 for Definition of Components)

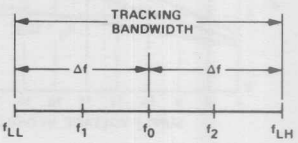
1. VCO Center Frequency, f_0:
   $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 10)
   $V_R = V+/2 - 650$ mV

3. Loop Low-Pass Filter Time Constant, τ:
   $\tau = R_1 C_1$

4. Loop Damping, ζ:
   $$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τ_F:
   $\tau_F = R_F C_F$

7. Loop Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input)
   $K_\phi = -2V_R/\pi$ volts/radian

8. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):
   $K_0 = -1/V_R C_0 R_1$ Hz/volt

9. Total Loop Gain, K_T:
   $K_T = 2\pi K_\phi K_0 = 4/C_0R_1$ rad/sec/volt

10. Peak Phase-Detector Current, I_A:
    $I_A = V_R$ (volts)/25 mA

APPLICATIONS INFORMATION

FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from Pin 7 to Pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table I.

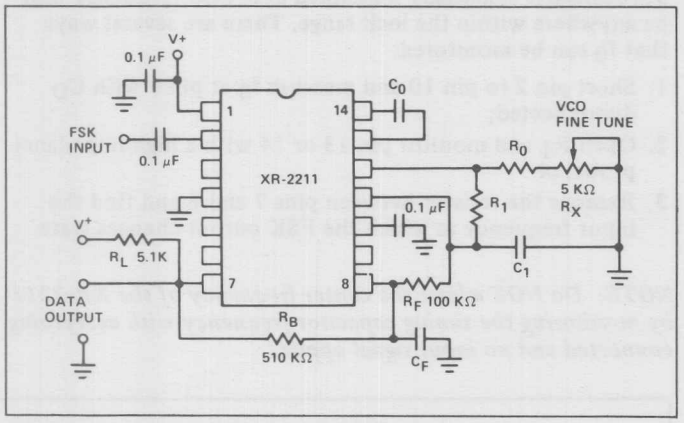


Figure 9. Circuit Connection for FSK Decoding

Design Instructions:

The circuit of Fig. 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_0:

$$f_0 = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Fig. 6:

$$C_0 = 1/R_0 f_0$$

d) Calculate R_1 to give a Δf equal to the mark-space deviation:

$$R_1 = R_0 [f_0/(f_1 - f_2)]$$

e) Calculate C_1 to set loop damping. (See Design Equation No. 4).

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

f) Calculate Data Filter Capacitance, C_F:

For R_F = 100 KΩ, R_B = 510 KΩ, the recommended value of C_F is:

$$C_F \approx 3/(\text{Baud Rate})\ \mu F$$

Note: All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Fig. 9).

Design Example:

75 Baud FSK demodulator with mark/space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: $f_0 = (1110 + 1170)(1/2) = 1140$ Hz
Step 2: Choose R_0 = 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer)
Step 3: Calculate C_0 from Fig. 6: $C_0 = 0.044\ \mu F$
Step 4: Calculate R_1: $R_1 = R_0 (2240/60) = 380$ KΩ
Step 5: Calculate C_1: $C_1 = C_0/4 = 0.011\ \mu F$

Note: All values except R_0 can be rounded-off to *nearest* standard value.

FSK BAND	COMPONENT VALUES	
300 Baud f_1 = 1070 Hz f_2 = 1270 Hz	$C_0 = 0.039\ \mu F$ $C_1 = 0.01\ \mu F$ R_1 = 100 KΩ	$C_F = 0.005\ \mu F$ R_0 = 18 KΩ
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	$C_0 = 0.022\ \mu F$ $C_1 = 0.0047\ \mu F$ R_1 = 200 KΩ	$C_F = 0.005\ \mu F$ R_0 = 18 KΩ
1200 Baud f_1 = 1200 Hz f_2 = 2200 Hz	$C_0 = 0.027\ \mu F$ $C_1 = 0.01\ \mu F$ R_1 = 30 KΩ	$C_F = 0.0022\ \mu F$ R_0 = 18 KΩ

TABLE I

Recommended Component Values for Commonly Used FSK Bands (See Circuit of Fig. 9)

FSK DECODING WITH CARRIER-DETECT:

The lock-detect section of XR-2211 can be used as a carrier-detect option, for FSK decoding. The recommended circuit connection for this application is shown in Fig. 10. The open-collector lock-detect output, Pin 6, is shorted to data. output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PPL, and the Pin 6 output goes "high", to enable the data output.

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_c > \Delta f/2$. For R_D = 470 KΩ, the approximate minimum value of C_D can be determined by:

$$C_D\ (\mu F) \geqslant 16/\text{capture range in Hz.}$$

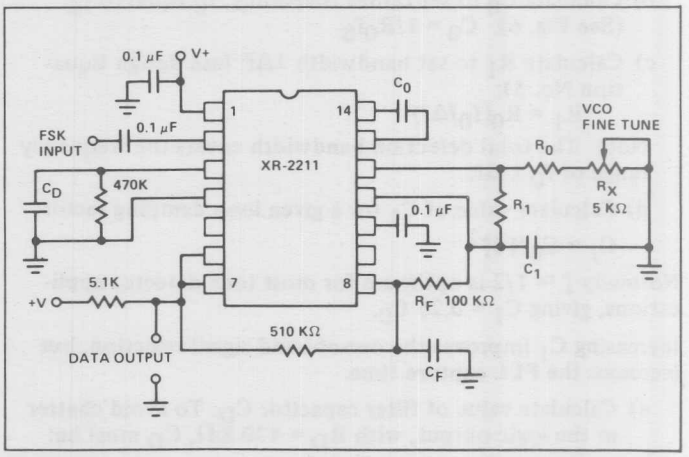


Figure 10. External Connectors for FSK Demodulation with Carrier-Detect Capability.
Note: Data Output is "Low" When No Carrier is Present.

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of C_D will slow the response time of the lock-detect output.

TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at Pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Fig. 11.

With reference to Figs. 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

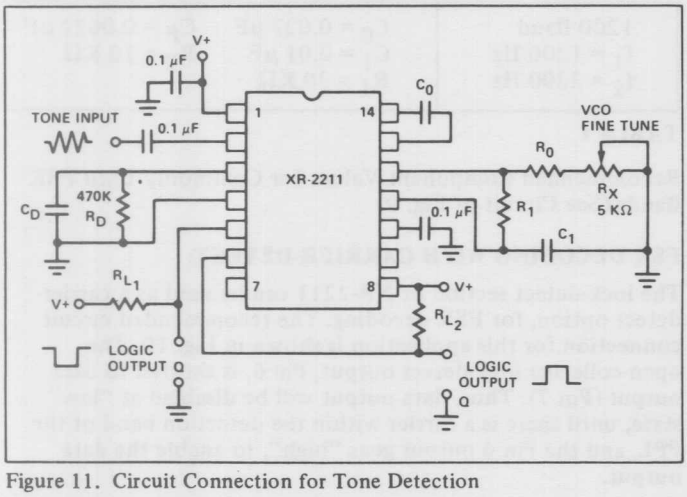


Figure 11. Circuit Connection for Tone Detection

Design Instructions:

The circuit of Fig. 11 can be optimized for any tone-detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15 KΩ.to 100 KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_S: (See Fig. 6). $C_0 = 1/R_0 f_S$

c) Calculate R_1 to set bandwidth ±Δf: (see design Equation No. 5):

$$R_1 = R_0(f_0/\Delta f)$$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor:

$$C_1 = C_0/16\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving $C_1 = 0.25\ C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470 KΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz ± 20 Hz:

a) Choose R_0 = 20 KΩ (18 KΩ in series with 5 KΩ potentiometer).
b) Choose C_0 for f_0 = 1 kHz: From Fig. 6: C_0 = 0.05 μF.
c) Calculate R_1: $R_1 = (R_0)(1000/20)$ = 1 MΩ.
d) Calculate C_1: for ζ = 1/2, C_1 = 0.25, C_0 = 0.013 μF.
e) Calculate C_D: C_D = 16/38 = 0.42 μF.
f) Fine-tune center frequency with 5 KΩ potentiometer, R_X.

ADJUSTMENT PROCEDURE

With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_0 can be monitored:

1. Short pin 2 to pin 10 and measure f_0 at pin 3 with C_D disconnected;
2. Open R_1 and monitor pin 13 or 14 with a high-impedance probe; or
3. Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

NOTE: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

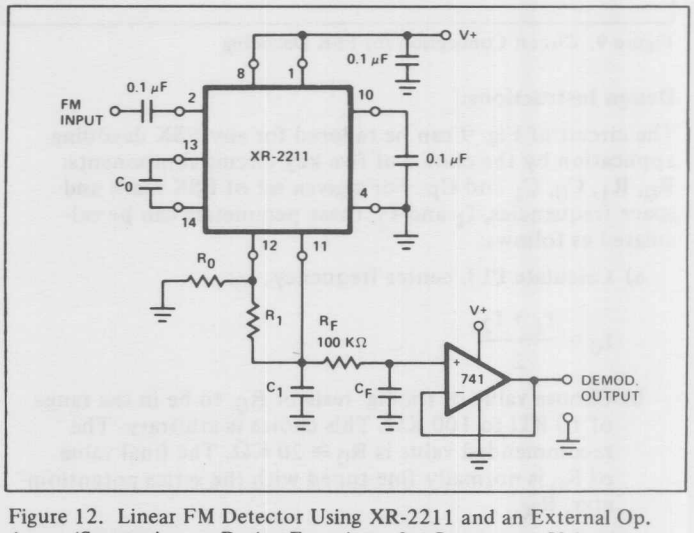


Figure 12. Linear FM Detector Using XR-2211 and an External Op. Amp. (See section on Design Equations, for Component Values)

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Fig. 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Fig. 12.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{out} = R_1\ V_R/100\ R_0\ \text{Volts/\%deviation}$$

where V_R is the internal reference voltage. (V_R = V+/2 – 650 mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on Design Equations.

XR-2212

Precision Phase-Locked Loop

FEBRUARY 1978

ADVANCE INFORMATION

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communication and control system applications. It offers 20 ppm/°C temperature stability and is ideally suited for frequency synthesis, FM detection and tracking filter applications. The circuit operates over a wide supply range of 4.5V to 20V, and a frequency range of 0.01 Hz to 300 kHz and can handle analog or digital signals from 2 mV to 6 volts, peak to peak.

The XR-2212 precision PLL is directly compatible with MOS, DTL and TTL logic families and microprocessor peripheral systems. The circuit consists of a PLL system made up of an input preamplifier, a phase detector, a stable voltage-controlled oscillator (VCO) and a high-gain differential amplifier. The VCO output is brought out externally so that the circuit can operate as a frequency synthesizer using an external programmable divider. The differential amplifier section can be used as an audio preamplifier for FM detection, or as a high-speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth and the tracking range of the PLL are controlled independently by the choice of external components.

FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, Typ.

APPLICATIONS

Frequency Synthesis
Data Synchronization
FM detection
Tracking Filters
FSK Demodulation

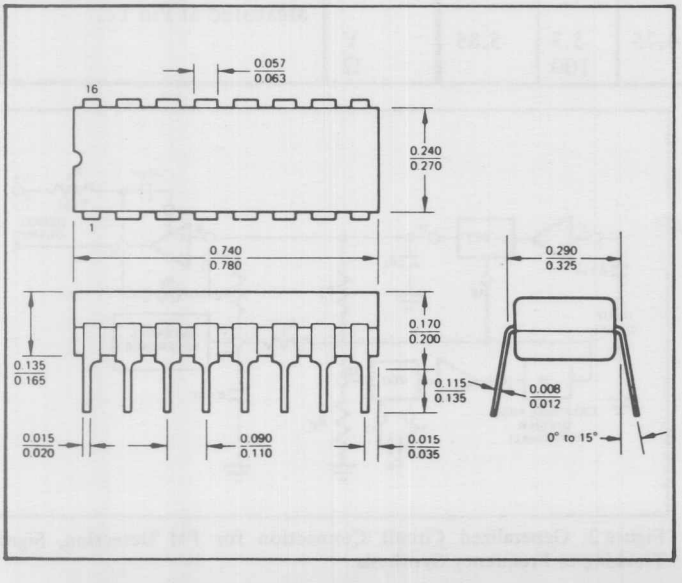
ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Input Signal Level	3 Vrms
Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5.0 mW/°C

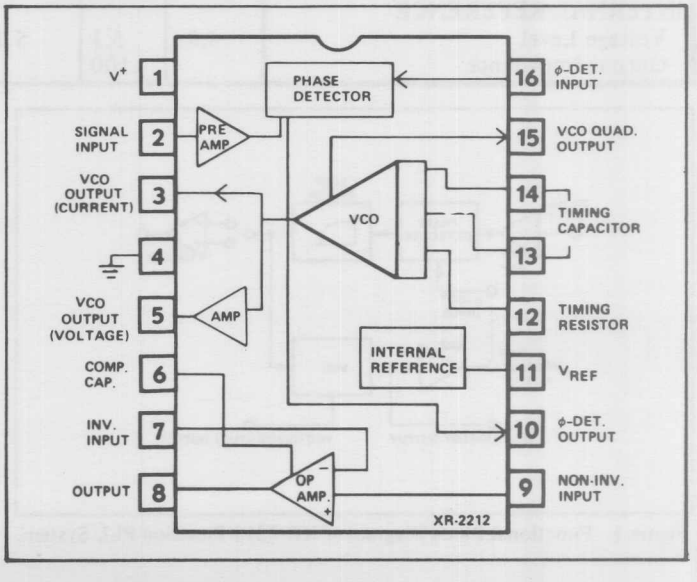
AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2212M	Ceramic	-55°C to +125°C
XR2212CN	Ceramic	0°C to +75°C
XR-2212CP	Plastic	0°C to +75°C
XR-2212N	Ceramic	-40°C to +85°C
XR-2212P	Plastic	-40°C to +85°C

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS – PRELIMINARY

Test Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30\ K\Omega$, $C_0 = 0.033\ \mu F$. See Fig. 2 for component designation.

CHARACTERISTICS	XR-2212/2212M			XR-2212C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL								
Supply Voltage	4.5		15	4.5		15	V	
Supply Current		6	10		6	12	mA	$R_0 \geqslant 10\ K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1V$. See Fig. 7.
		.2			.2		%/V	$V^+ = 5 \pm 0.5V$. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ K\Omega$, $C_0 = 400\ pF$
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
OSCILLATOR OUTPUTS								
Voltage Output								Measured at Pin 5.
Positive Swing, V_{OH}		11			11		V	
Negative Swing, V_{OL}	.8	.4			.5		V	
Current Sink Capability		1			1		mA	
Current Output								Measured at Pin 3.
Peak Current Swing	100	150			150		μA	
Output Impedance		1			1		MΩ	
Quadrature Output								Measured at Pin 15.
Output Swing		0.6			0.6		V	
DC Level		0.3			0.3		V	Referenced to Pin 11.
Output Impedance		3			3		KΩ	
LOOP PHASE DETECTOR SECTION								Measured at Pin 10.
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 11.
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		KΩ	
Input Signal to Cause Limiting		2	10		2		mVrms	
OP AMP SECTION								
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ K\Omega$, $R_F = \infty$
Input Bias Current		0.1	1		0.1	1	μA	
Offset Voltage		±5	±20		±5	±20	mV	
Slew Rate		2			2		V/μsec	
INTERNAL REFERENCE								Measured at Pin 11.
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	
Output Impedance		100			100		Ω	

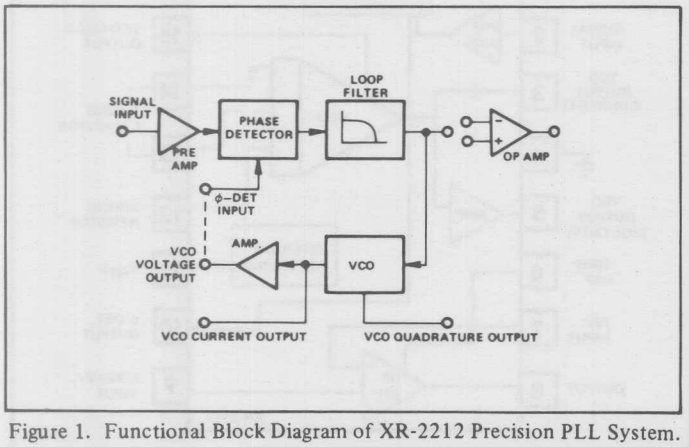


Figure 1. Functional Block Diagram of XR-2212 Precision PLL System.

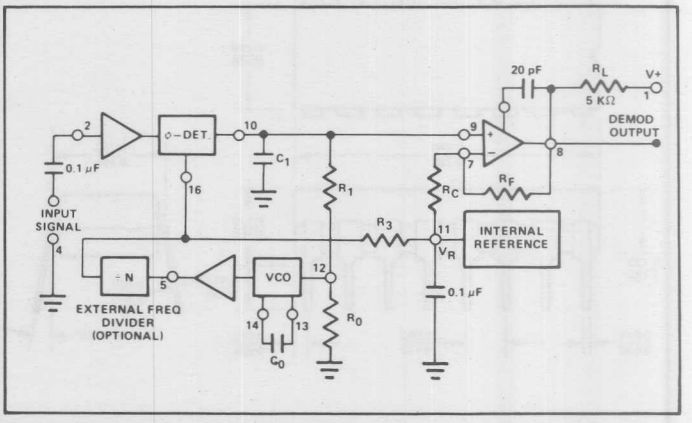


Figure 2. Generalized Circuit Connection for FM Detection, Signal Tracking or Frequency Synthesis.

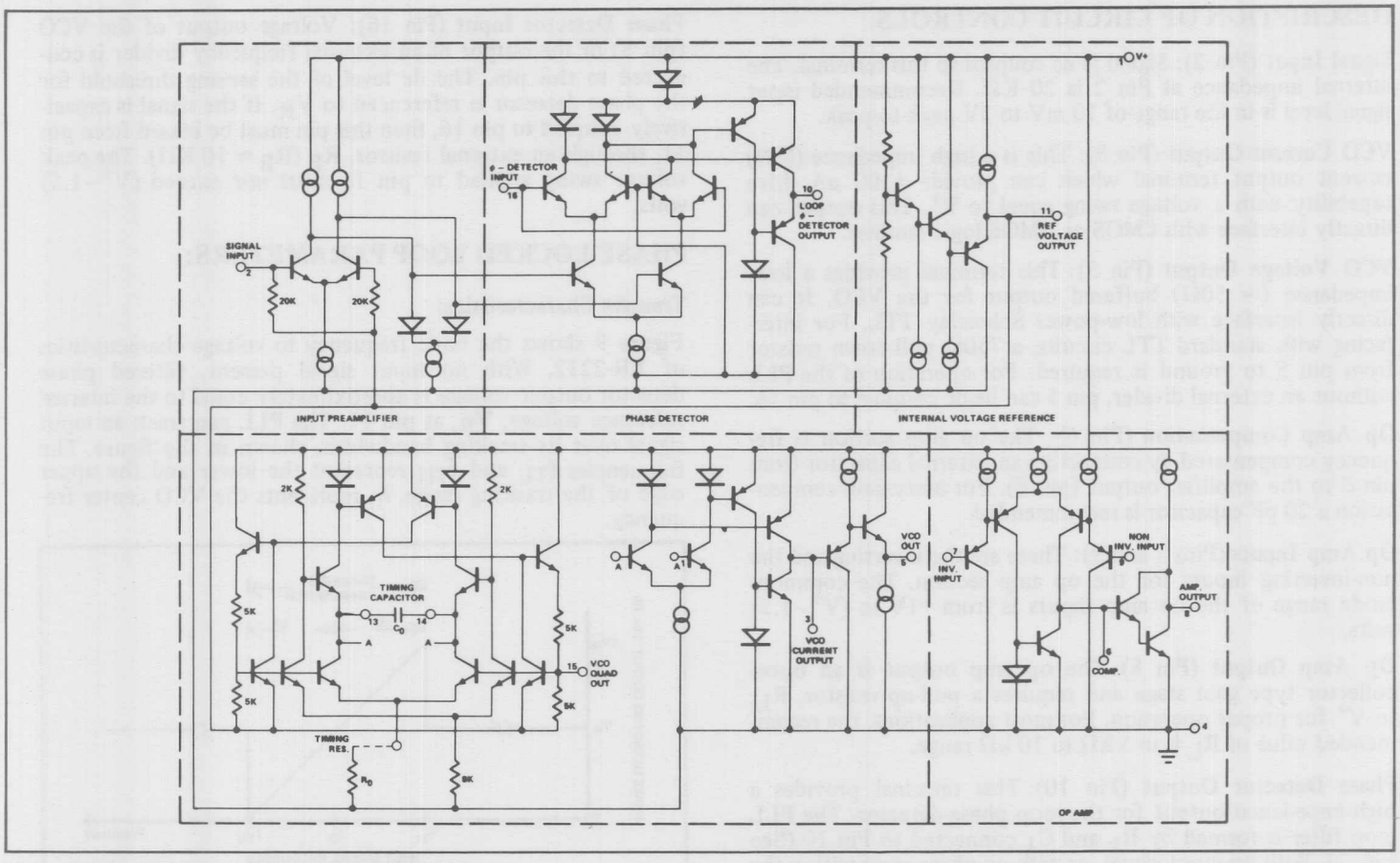


Figure 3. Simplified Circuit Schematic of XR-2212.

TYPICAL CHARACTERISTICS

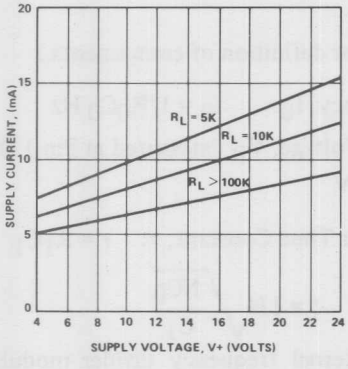


Figure 4. Typical Supply Current vs V^+ (Logic Outputs Open Circuited).

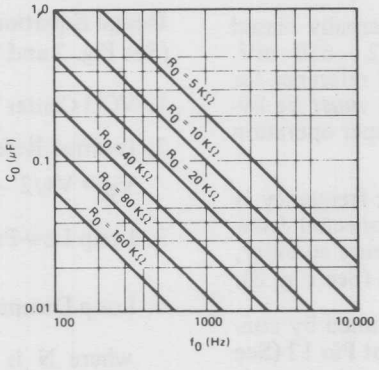


Figure 5. VCO Frequency vs Timing Resistor

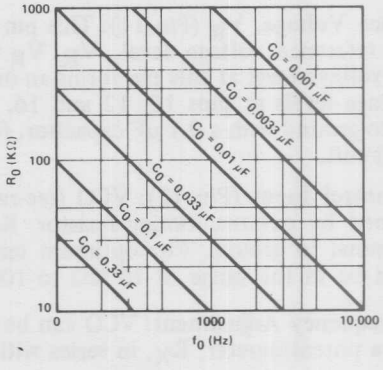


Figure 6. VCO Frequency vs Timing Capacitor

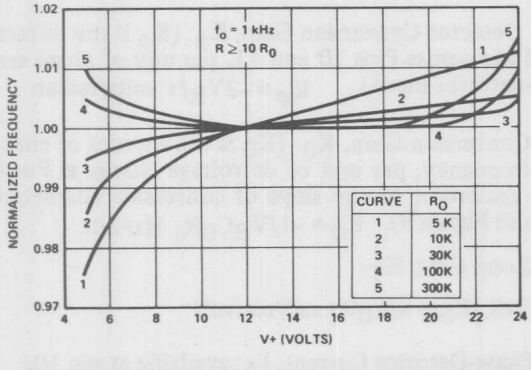


Figure 7. Typical f_0 vs Power Supply Characteristics.

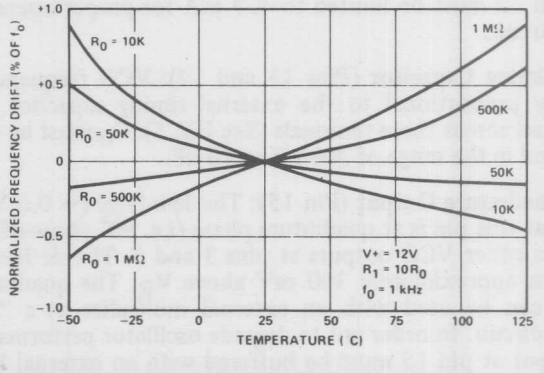


Figure 8. Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV to 5V peak-to-peak.

VCO Current Output (Pin 3): This is a high impedance (MΩ) current output terminal which can provide ±100 μA drive capability with a voltage swing equal to V^+. This output can directly interface with CMOS or NMOS logic families.

VCO Voltage Output (Pin 5): This terminal provides a low-impedance (≈ 50Ω) buffered output for the VCO. It can directly interface with low-power Schottley TTL. For interfacing with standard TTL circuits, a 750Ω pull-down resistor from pin 5 to ground is required. For operation of the PLL without an external divider, pin 5 can be dc coupled to pin 16.

Op Amp Compensation (Pin 6): The op amp section is frequency compensated by connecting an external capacitor from pin 6 to the amplifier output (pin 8). For unity-gain compensation a 20 pF capacitor is recommended.

Op Amp Inputs (Pins 7 and 9): These are the inverting and the non-inverting inputs for the op amp section. The common-mode range of the op amp inputs is from +1V to (V^+–1.5) volts.

Op Amp Output (Pin 8): The op amp output is an open-collector type gain stage and requires a pull-up resistor, R_L, to V^+ for proper operation. For most applications, the recommended value of R_L is in 5 kΩ to 10 kΩ range.

Phase Detector Output (Pin 10): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 10 (See Fig. 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 10 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

Reference Voltage, V_R (Pin 11): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 10, 12 and 16. Pin 1 *must* be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ (See Fig. 8).

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (See Fig. 10).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ⩽ 3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (See Fig. 5). C_0 must be non-polar, and in the range of 200 pF to 10 μF.

VCO Quadrature Output (Pin 15): The low-level (≈ 0.6 Vpp) output at this pin is at quadrature phase (i.e. 90° phase-offset) with the other VCO outputs at pins 3 and 5. The dc level at pin 15 is approximately 300 mV above V_R. The quadrature output can be used with an external multiplier as a "lock detect" circuit. In order not to degrade oscillator performance, the output at pin 15 must be buffered with an external high-impedance low-capacitance amplifier. When not in use, pin 15 should be left open-circuited.

Phase Detector Input (Pin 16): Voltage output of the VCO (pin 5) or the output of an external frequency divider is connected to this pin. The dc level of the sensing threshold for the phase detector is referenced to V_R. If the signal is capacitively coupled to pin 16, then this pin must be biased from pin 11, through an external resistor, R_B ($R_B \approx 10$ KΩ). The peak voltage swing applied to pin 16 *must not* exceed (V^+–1.5) volts.

PHASE-LOCKED LOOP PARAMETERS:

Transfer Characteristics:

Figure 9 shows the basic frequency to voltage characteristics of XR-2212. With no input signal present, filtered phase detector output voltage is approximately equal to the internal reference voltage, V_R, at pin 11. The PLL can track an input signal over its tracking bandwidth, shown in the figure. The frequencies f_{TL} and f_{TH} represent the lower and the upper edge of the tracking range, f_0 represents the VCO center frequency.

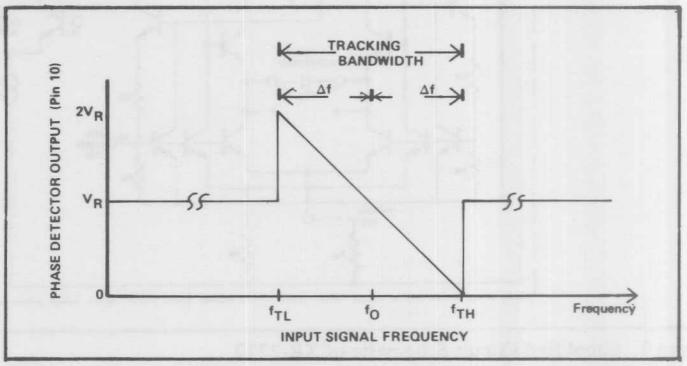


Figure 9. Phase detector output voltage (pin 10) as a function of input signal frequency. Note: Output voltage is referenced to internal reference voltage V_R at pin 11.

Design Equations:

(See Fig. 2 and Fig. 9 for definition of components.)

1. VCO Center Frequency, f_0: $f_0 = 1/R_0C_0$ Hz
2. Internal Reference Voltage, V_R (measured at Pin 11)
   $V_R = V+/2 - 650$ mV
3. Loop Low-Pass Filter Time Constant, τ: $\tau = R_1C_1$
4. Loop Damping, ζ: $\zeta = 1/4\sqrt{\frac{NC_0}{C_1}}$
   where N is the external frequency divider modular (See 2). If no divider is used, N = 1.
5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$: $\Delta f/f_0 = R_0/R_1$
6. Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input) $K_\phi = -2V_R/\pi$ volts/radian
7. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 10. It is the reciprocal of the slope of conversion characteristics shown in Figure 9). $K_0 = -1/V_RC_0R_1$ Hz/volt
8. Total Loop Gain, K_T:
   $K_T = 2\pi K_\phi K_0 = 4/C_0R_1$ rad/sec/volt
9. Peak Phase-Detector Current, I_A; available at pin 10.
   $I_A = V_R$ (volts)/25 mA

APPLICATION INFORMATION

FM DEMODULATION:

XR-2212 can be used as a linear FM demodulator for both narrow-band and wide-band FM signals. The generalized circuit connection for this application is shown in Fig. 10, where the VCO output (pin 5) is directly connected to the phase detector input (pin 16). The demodulated signal is obtained at phase detector output (pin 10). In the circuit connection of Fig. 10, the op amp section of XR-2212 is used as a buffer amplifier to provide both additional voltage amplification as well as current drive capability. Thus, the demodulated output signal available at the op amp output (pin 8) is fully buffered from the rest of the circuit.

In the circuit of Fig. 10, R_0C_0 set the VCO center frequency, R_1 sets the tracking bandwidth, C_1 sets the low-pass filter time constant. Op amp feedback resistors R_F and R_C set the voltage gain of the amplifier section.

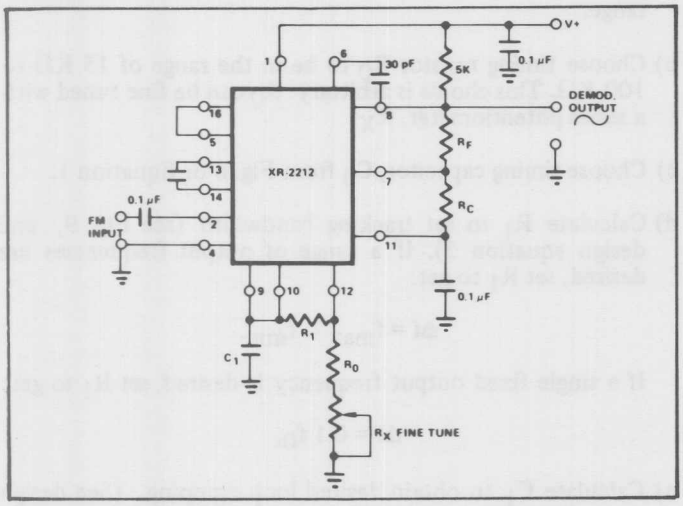


Figure 10. Circuit Connection for FM Demodulation.

Design Instructions:

The circuit of Fig. 10 can be tailored to any FM demodulation application by a choice of the external components R_0, R_1, R_C, R_F, C_0 and C_1. For a given FM center frequency and frequency deviation, the choice of these components can be calculated as follows, using the design equations and definitions given on page 4:

a) Choose VCO center frequency f_0 to be the same as FM carrier frequency.

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Fig. 6:

$$C_0 = 1/R_0 f_0$$

d) Choose R_1 to determine the tracking bandwidth, Δf (see design equation 5). The tracking bandwidth, Δf, should be set significantly wider than the maximum input FM signal deviation, Δf_{SM}. Assuming the tracking bandwidth to be "N" times larger than Δf_{SM}, one can re-unite design equation 5 as:

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1} = N \frac{\Delta f_{SM}}{f_0}$$

Table I lists recommended values of N, for various values of the maximum deviation of the input FM signal.

e) Calculate C_1 to set loop damping (see design equation 4). Normally, $\zeta = 1/2$ is recommended. Then, $C_1 = C_0/4$ for $\zeta = 1/2$.

% Deviation of FM Signal ($\Delta f_{SM}/f_0$)	Recommended value of Bandwidth Ratio, N ($N = \Delta f/\Delta f_{SM}$)
1% or less	10
1 to 3%	5
1 to 5%	4
5 to 10%	3
10 to 30%	2
30 to 50%	1.5

TABLE I

Recommended values of bandwidth ratio, N, for various values of FM signal frequency deviation. (Note: N is the ratio of tracking bandwidth Δf to max. signal frequency deviation, Δf_{SM}).

f) Calculate R_C and R_F to set peak output signal amplitude. Output signal amplitude, V_{out}, is given as:

$$V_{out} = \left(\frac{\Delta f_{SM}}{f_0}\right)\left(V_R\right)\left(\frac{R_1}{R_0}\right)\left[\frac{R_C + R_F}{R_C}\right]$$

In most applications, $R_F = 100$ KΩ is recommended; then R_C, can be calculated from the above equation to give desired output swing. The output amplifier can also be used as a unity-gain voltage follower, by open circuiting R_C (i.e., $R_C = \infty$).

Note: All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Fig. 10.)

Design Example:

Demodulator for FM signal with 67 kHz carrier frequency with ±5 kHz frequency deviation. Supply voltage is +12V and required peak output swing is ±4 volts.

Step a) f_0 is chosen as 67 kHz.

Step b) Choose R_0 = 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer).

Step c) Calculate C_0; from design Eq. (1).

$C_0 = 746$ pF

Step d) Calculate R_1. For given FM deviation, $\Delta f_{SM}/f_0 = 0.0746$, and N = 3 from Table I.

Then:

$R_0/R_1 = (3)(0.0746) = 0.224$

or:

$R_1 = 89.3$ KΩ.

Step e): Calculate $C_1 = (C_0/4) = 186$ pF.

Step f: Calculate R_C and R_F to get ±4 volts peak output swing: Let $R_F = 100$ KΩ. Then,

$R_C = 80.6$ KΩ.

Note: All values except R_0 can be rounded-off to nearest standard value.

FREQUENCY SYNTHESIS

Fig. 11 shows the generalized circuit connection for frequency synthesis. In this application an external frequency divider is connected between the VCO output (pin 5) and the phase-detector input (pin 16). When the circuit is in lock, the two signals going into the phase-detector are at the same frequency, or $f_S = f_1/N$ where N is the modulus of the external frequency divider. Conversely, the VCO output frequency, f_1 is equal to Nf_S.

In the circuit configuration of Fig. 11, the external timing components, R_0 and C_0, set the VCO free-running frequency; R_1 sets the tracking bandwidth and C1 sets the loop damping, i.e., the low-pass filter time constant (see design equations).

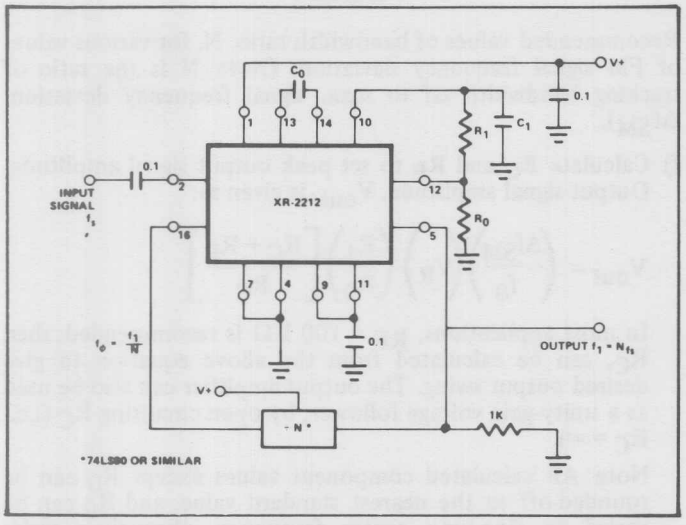


Figure 11. Circuit Connection for Frequency Synthesizer.

The total tracking range of the PLL (see Fig. 9), should be chosen to accomodate the lowest and the highest frequency, f_{max} and f_{min}, to be synthesized. A recommended choice for most applications is to choose a tracking half-bandwidth Δf, such that:

$$\Delta f \approx f_{max} - f_{min}.$$

If a fixed output frequency is desired, i.e. N and f_S are fixed, then a ±10% tracking bandwidth is recommended. Excessively large tracking bandwidth may cause the PLL to lock on the harmonics of the input signals; and the small tracking range increases the "lock-up" or acquisition time.

If a variable input frequency and a variable counter modulus N is used, then the maximum and the minimum values of output frequency will be:

$$f_{max} = N_{max}\,(f_S)_{max} \text{ and } f_{min} = N_{min}\,(f_S)_{min}.$$

Design Instructions:

For a given performance requirement, the circuit of Fig. 11 can be optimized as follows:

a) Choose center frequency, f_0, to be equal to the output frequency to be synthesized. If a range of output frequencies is desired, set f_0 to be at mid-point of the desired range.

b) Choose timing resistor R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary. R_0 can be fine tuned with a series potentiometer, R_X.

c) Choose timing capacitor, C_0 from Fig. 6 or Equation 1.

d) Calculate R_1 to set tracking bandwidth (see Fig. 9, and design equation 5). If a range of output frequencies are desired, set R_1 to get:

$$\Delta f = f_{max} - f_{min}.$$

If a single fixed output frequency is desired, set R_1 to get:

$$\Delta f = 0.1\, f_0.$$

e) Calculate C_1 to obtain desired loop damping. (See design equation 4). For most applications, $\zeta = 1/2$ is recommended, thus:

$$C_0 = NC_0/4$$

Note: All component values except R_0 can be rounded-off to nearest standard value.

XR-567

Monolithic Tone Decoder

August 1972

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01 Hz to 500 kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

Figure 1 contains a functional block diagram of the complete monolithic system. The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enable the system to distinguish between the presence or absence of an input signal at the center frequency.

FEATURES

Bandwidth adjustable from 0 to 14%.

Logic compatible output with 100 mA current sinking capability.

Highly stable center frequency.

Center frequency adjustable from 0.01 Hz to 500 kHz.

Inherent immunity to false signals.

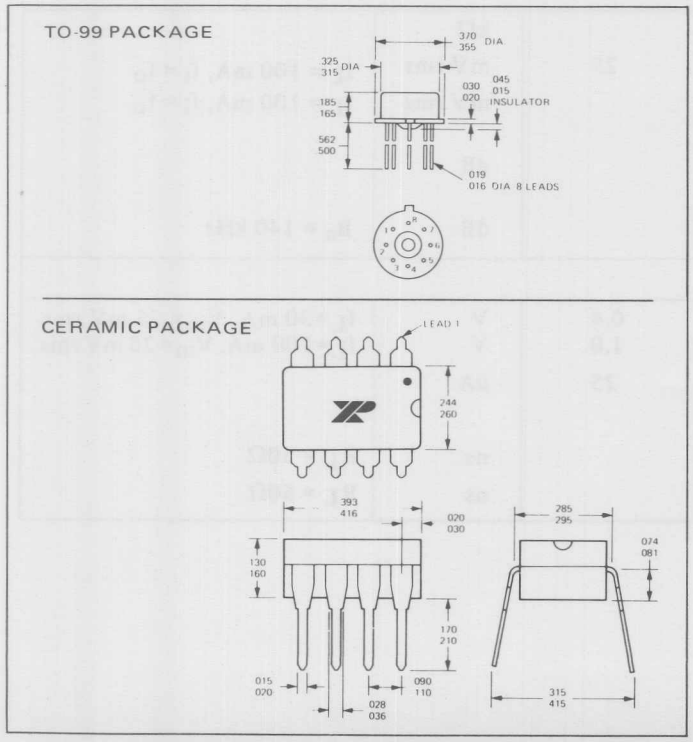
High rejection of out-of-band signals and noise.

Frequency range adjustable over 20:1 range by external resistor.

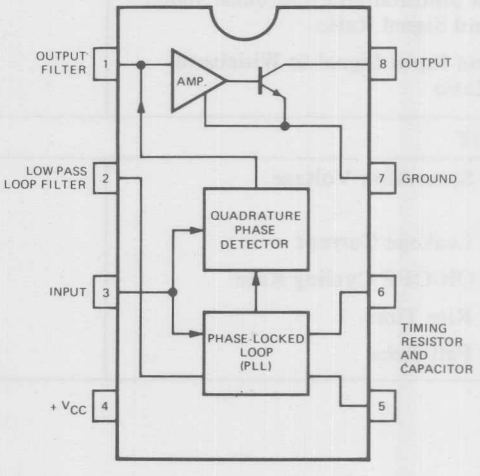
ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic package	385 mW
Derate above +25°C	5.0 mW/°C
TO-99 Metal can	680 mW
Derate above +25°C	4.6 mW/°C
Temperature	
Operating	
XR-567N/567T	–55°C to +125°C
XR-567CN/567CT	0° to +70°C
Storage	–65°C to +150°C

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM



(Same pinouts for TO-99 package)

Figure 1 Functional Block Diagram

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test circuit of Figure 2.

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN	TYP	MAX		
GENERAL					
Supply Voltage Range	4.75		9.0	V dc	
Supply Current					
Quiescent XR-567		6	8	mA	R_L = 20 kΩ
XR-567C		7	10	mA	R_L = 20 kΩ
Activated XR-567		11	13	mA	R_L = 20 kΩ
XR-567C		12	15	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 9
0 < T_A < 70°C		±60		ppm/°C	See Figure 9
−55 < T_A < +125°C		±140		ppm/°C	See Figure 9
Supply Voltage					
XR-567		0.5	1.0	%/V	f_o = 100 kHz
XR-567C		0.7	2.0	%/V	f_o = 100 kHz
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567	12	14	16	% of f_o	f_o = 100 kHz
XR-567C	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR-567		1	2	% of f_o	
XR-567C		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140 kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L=30 mA, V_{in}= 25 mV rms
		0.6	1.0	V	I_L=100 mA, V_{in}=25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

DEFINITION OF XR-567 PARAMETERS

CENTER FREQUENCY f_o

f_o is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground. f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

DETECTION BANDWIDTH (BW)

The *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_o, can be determined by the approximation

$$BW = 1070\sqrt{\frac{V_i}{f_o C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

LARGEST DETECTION BANDWIDTH

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BAND SKEW

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls).

DESCRIPTION OF CIRCUIT CONTROLS

OUTPUT FILTER – C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass *post detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7 kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be $\geq 2\ C_2$, where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the *turn-on* or *turn-off* time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector (see Figure 1) may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

LOOP FILTER – C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-567. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 6. For additional information see section on "Definition of XR-567 Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squareware output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

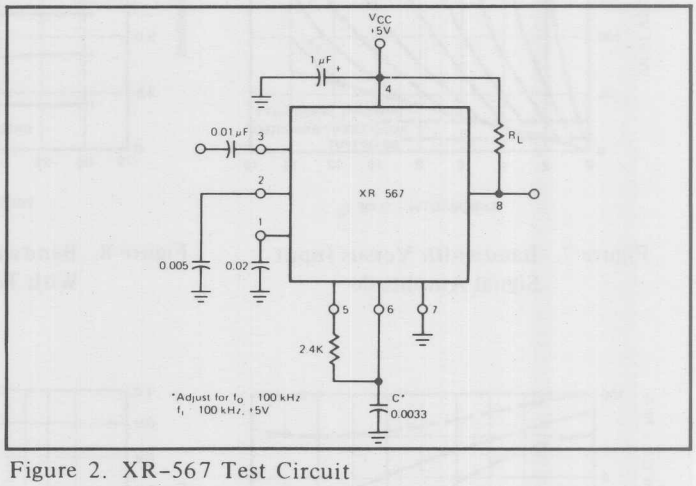


Figure 2. XR-567 Test Circuit

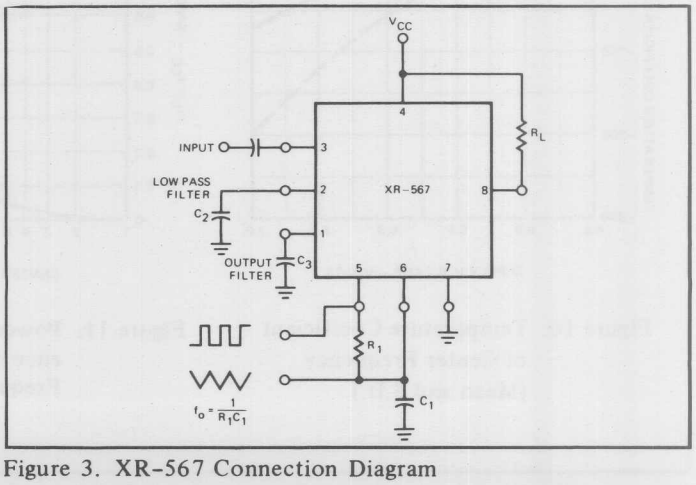


Figure 3. XR-567 Connection Diagram

TYPICAL CHARACTERISTIC CURVES

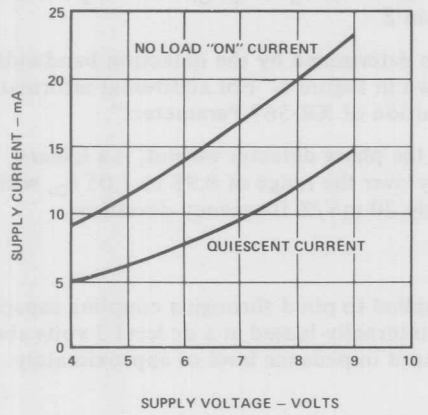


Figure 4. Supply Current Versus Supply Voltage

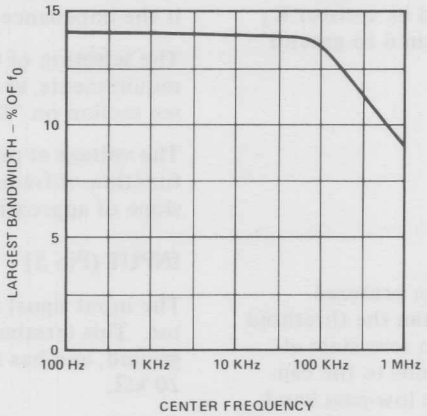


Figure 5. Largest Detection Bandwidth Versus Operating Frequency

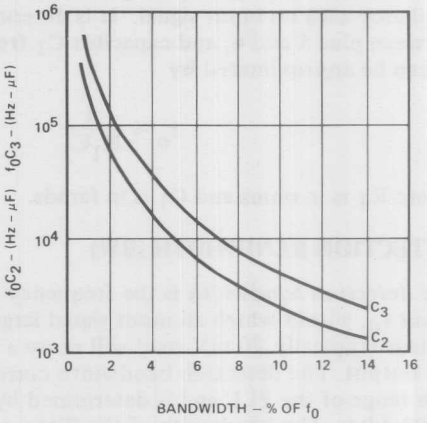


Figure 6. Detection Bandwidth as a Function of C_2 and C_3

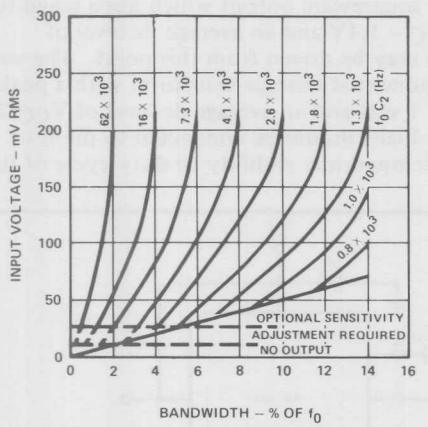


Figure 7. Bandwidth Versus Input Signal Amplitude

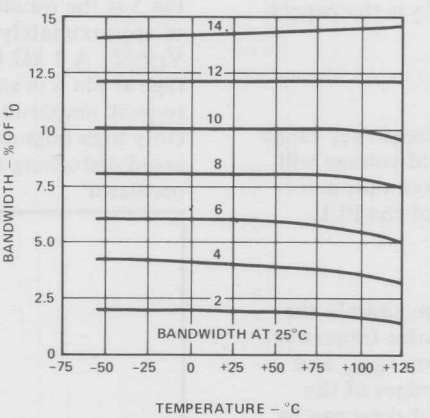


Figure 8. Bandwidth Variation With Temperature

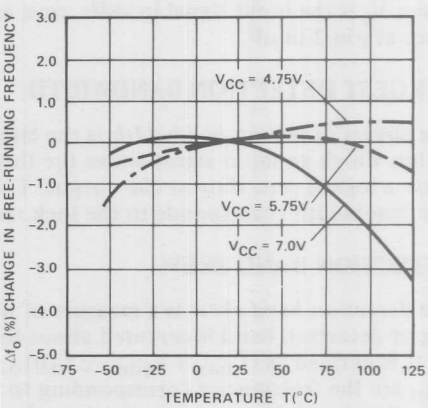


Figure 9. Frequency Drift With Temperature

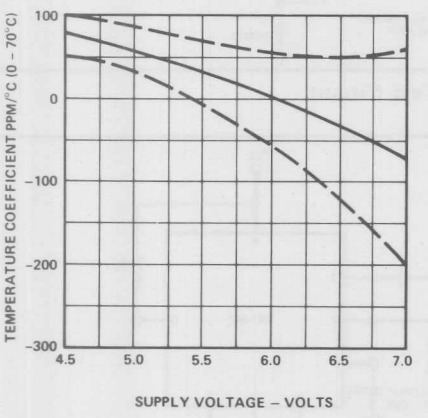


Figure 10. Temperature Coefficient of Center Frequency (Mean and S.D.)

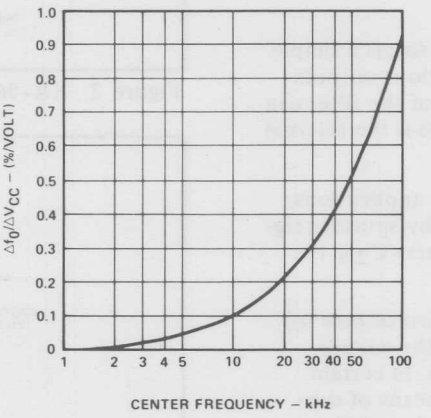


Figure 11. Power Supply Dependence of Center Frequency

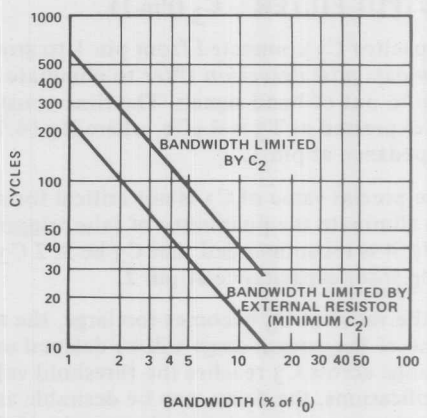


Figure 12. Greatest Number of Cycles Before Output

LOGIC OUTPUT (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "bare-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, $V+ \leq 20$ volts.

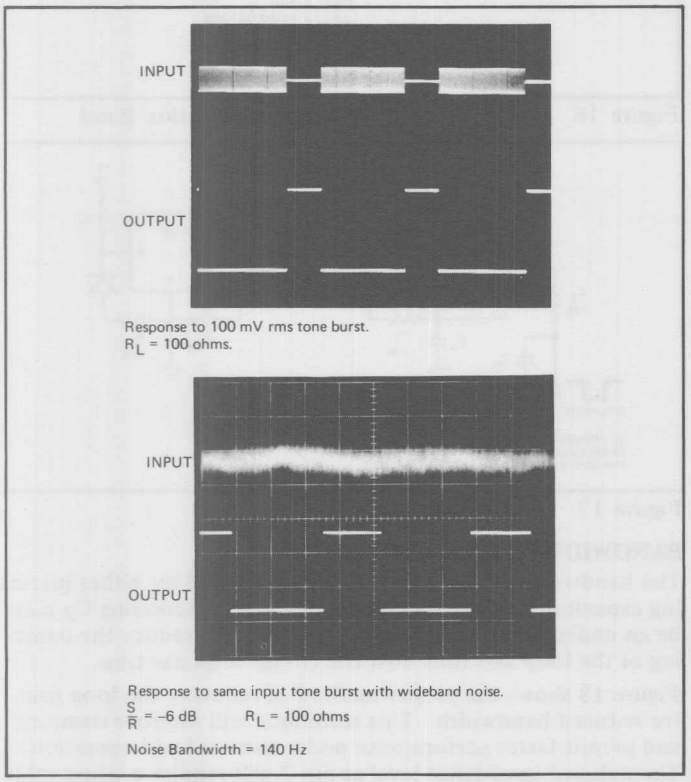


Figure 13. Typical Response

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the XR-567 is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that $2\Omega \leq R_1 \leq 20\Omega$, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200$ mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.
3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C_3 is $2\,C_2$.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The XR-567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3.

OPTIONAL CONTROLS

PROGRAMMING

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}, \quad C_3 = \frac{260}{f_o}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 14 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

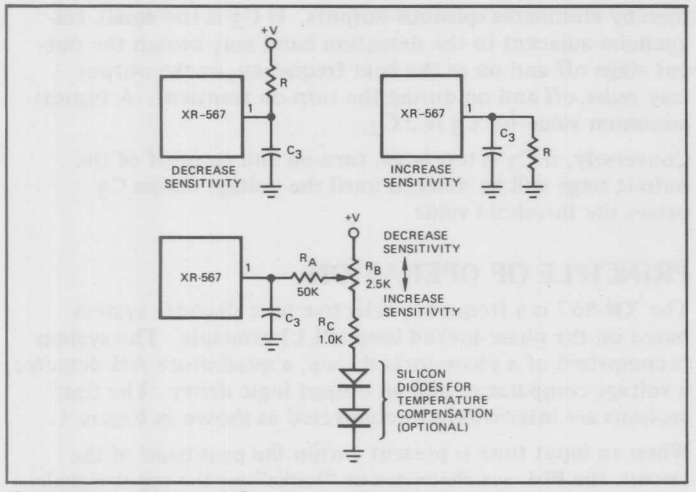


Figure 14. Optional Sensitivity Connections

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 15. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

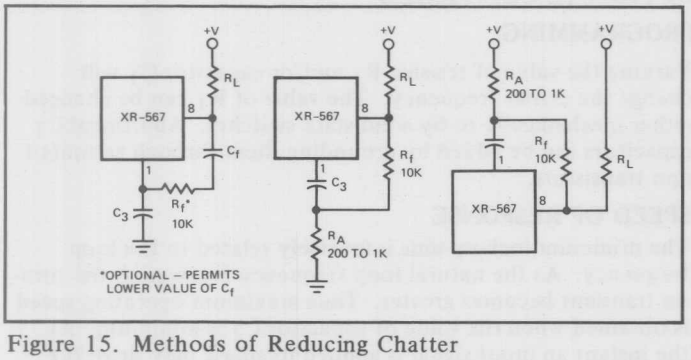


Figure 15. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Figure 16 can be used to change the position of the detection band (capture range) within the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

OUTPUT LATCHING

In order to latch the output of the XR-567 "on" after a signal is received, it is necessary to include a feedback resistor around the output stage, between pin 8 and pin 1, as shown in Figure 17. Pin 1 is pulled up to unlatch the output stage.

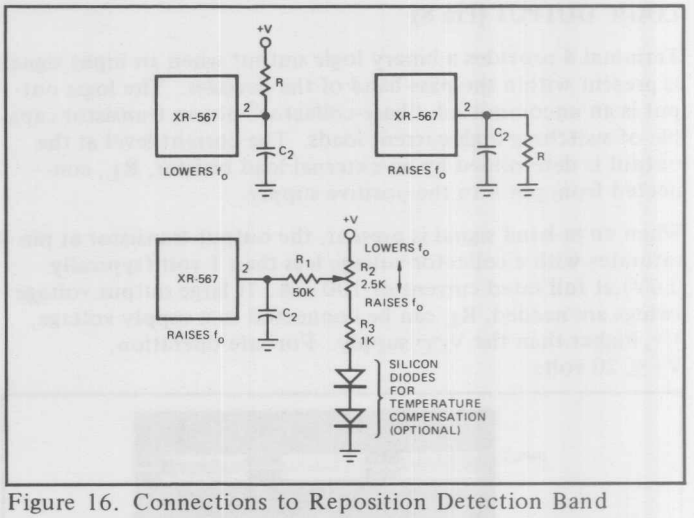


Figure 16. Connections to Reposition Detection Band

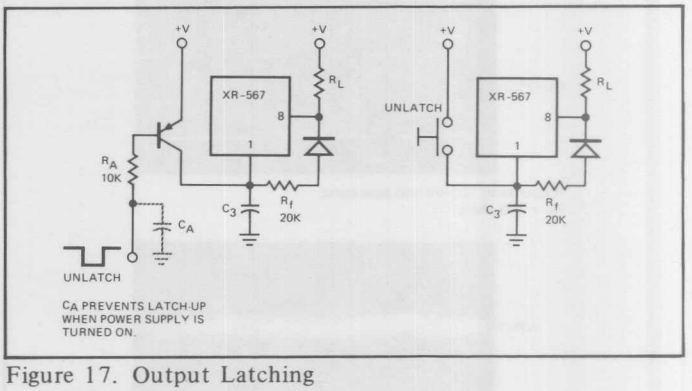


Figure 17. Output Latching

BANDWIDTH REDUCTION

The bandwidth of the XR-567 can be reduced by either increasing capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 18 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. The reduced impedance level at pin 2 will require a larger value of C_2 for a given cutoff frequency.

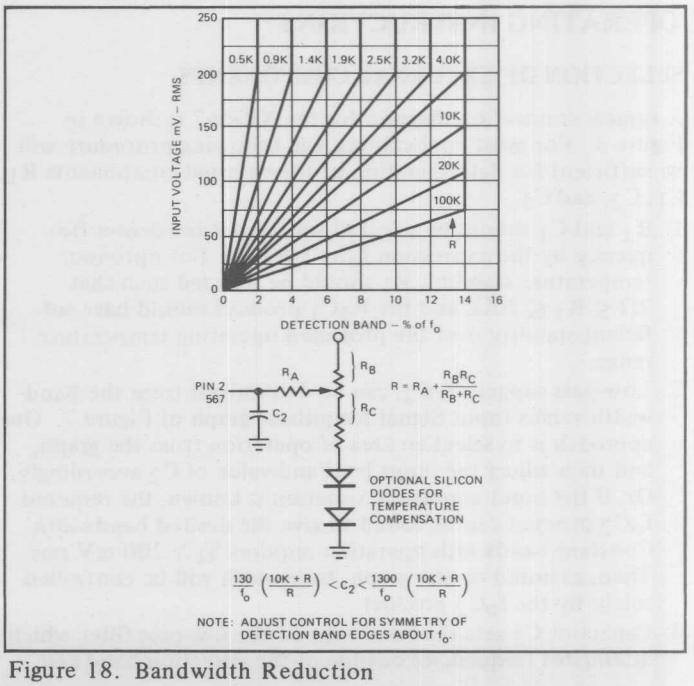


Figure 18. Bandwidth Reduction

PRECAUTIONS

1. The XR-567 will lock on signals near $(2n + 1)\ f_o$ and produce an output for signals near $(4n + 1)\ f_o$, for $n = 0,1,2$ – etc. Signals at $5\ f_o$ and $9\ f_o$ can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-567 in a reduced bandwidth mode of operation at input levels less than 200 mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 12.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-567 in the high input level mode, above 200 mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create inband components from sub-harmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

ADDITIONAL APPLICATIONS

DUAL TIME CONSTANT TONE DECODER

For some applications it is important to have a tone decoder with narrow bandwidth and fast response time. This can be accomplished by the dual time constant tone decoder circuit shown in Figure 19. The circuit has two low-pass loop filter capacitors, C_2 and C'_2. With no input signal present, the output at pin 8 is high, transistor Q_1 is off, and C'_2 is switched out of the circuit. Thus the loop low-pass filter is comprised of C_2, which can be kept as small as possible for minimum response time.

When an in-band signal is detected, the output at pin 8 will go low, Q_1 will turn on, and capacitor C'_2 will be switched in parallel with capacitor C_2. The low-pass filter capacitance will then be $C_2 + C'_2$. The value of C'_2 can be quite large in order to achieve narrow bandwidth. Notice that during the time that no input signal is being received, the bandwidth is determined by capacitor C_2.

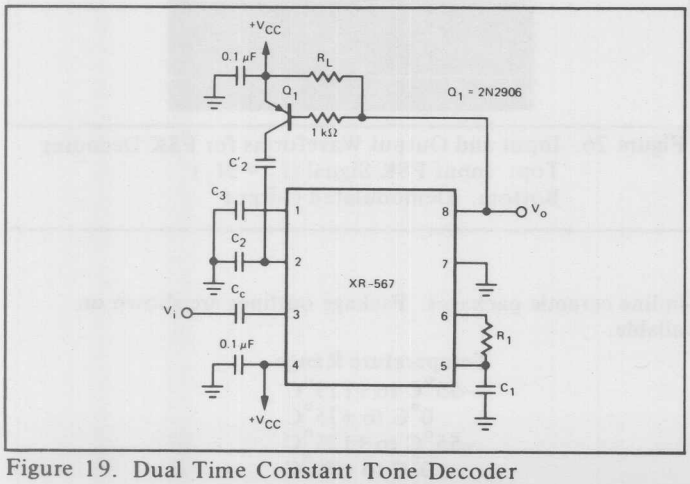


Figure 19. Dual Time Constant Tone Decoder

NARROW BAND FM DEMODULATOR WITH CARRIER DETECT

For FM demodulation applications where the bandwidth is less than 10% of the carrier frequency, and XR-567 can be used to detect the presence of the carrier signal. The output of the XR-567 is used to turn off the FM demodulator when no carrier is present, thus acting as a squelch. In the circuit shown, an XR-215 FM demodulator is used because of its wide dynamic range, high signal/noise ratio and low distortion. The XR-567 will detect the presence of a carrier at frequencies up to 500 kHz.

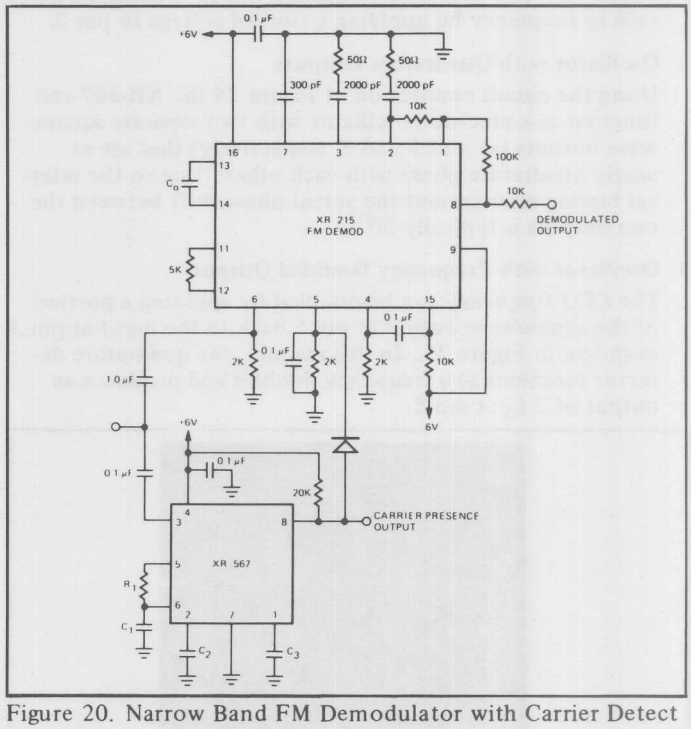


Figure 20. Narrow Band FM Demodulator with Carrier Detect

DUAL TONE DECODER

In dual tone communication systems, information is transmitted by the simultaneous presence of two separate tones at the input. In such applications two XR-567 units can be connected in parallel, as shown in Figure 21 to form a dual tone decoder. The resistor and capacitor values of each decoder are selected to provide the desired center frequencies and bandwidth requirements.

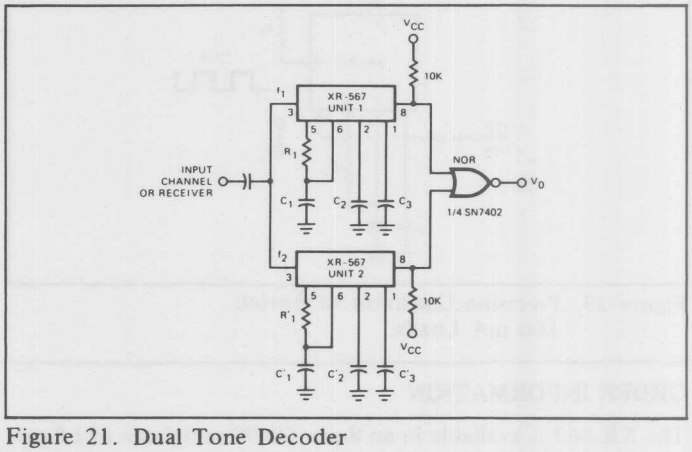


Figure 21. Dual Tone Decoder

PRECISION OSCILLATOR

The current-controlled oscillator (CCO) section of the XR-567 provides two basic output waveforms as shown in Figure 22. The squarewave is obtained from pin 5, and the exponential ramp from pin 6. The relative phase relationships of the wave-

forms are also provided in the figure. In addition to being used as a general purpose oscillator or clock generator, the CCO can also be used for any of the following special purpose oscillator applications:

1. **High-Current Oscillator**

   The oscillator output of the XR-567 can be amplified using the output amplifier and high-current logic output available at pin 8. In this manner, the circuit can switch 100 mA load currents without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 23. The oscillator frequency can be modulated over ±6% in frequency by applying a control voltage to pin 2.

2. **Oscillator with Quadrature Outputs**

   Using the circuit connection of Figure 24 the XR-567 can function as a precision oscillator with two separate squarewave outputs (at pins 5 and 8, respectively) that are at nearly quadrature phase with each other. Due to the internal biasing arrangement the actual phase shift between the two outputs is typically 80°.

3. **Oscillator with Frequency Doubled Output**

   The CCO frequency can be doubled by applying a portion of the squarewave output at pin 5 back to the input at pin 3, as shown in Figure 25. In this manner, the quadrature detector functions as a frequency doubler and produces an output of 2 f_o at pin 8.

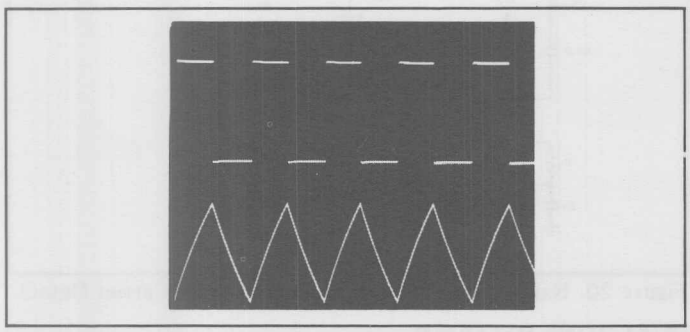


Figure 22. Oscillator Output Waveform Available From CCO Section.
Top: Square Wave Output at Pin 5:
Amplitude = $(V^+ - 1.4V)$, pp., Avg. Value = $V^+/2$
Bottom: Exponential Triangle Wave at Pin 6:
Amplitude = 1 V pp., Avg. Value = $V^+/2$

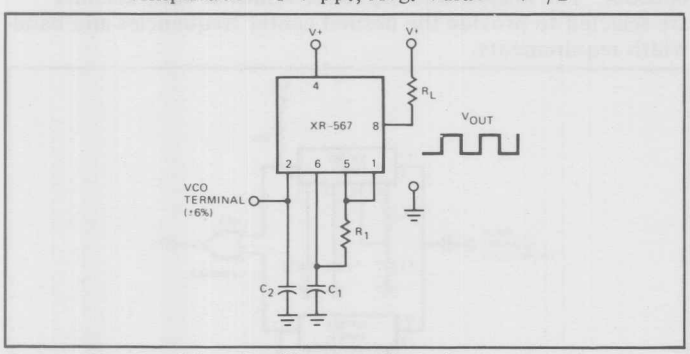


Figure 23. Precision Oscillator to Switch 100 mA Loads

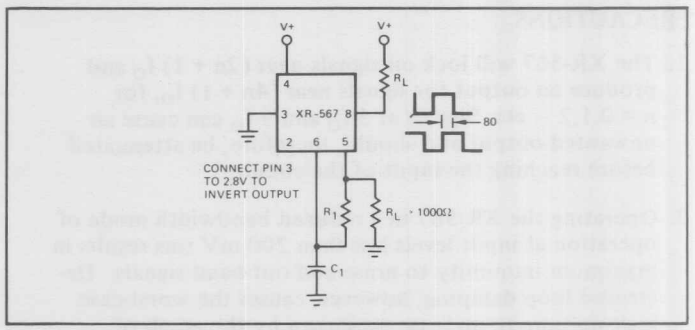


Figure 24. Oscillator with Quadrature Output

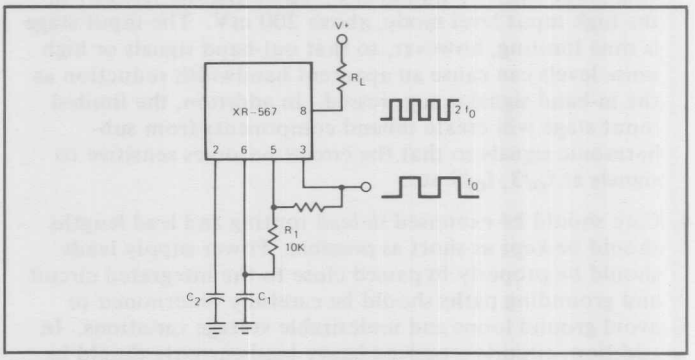


Figure 25. Oscillator with Double Frequency Output

FSK DECODING

XR-567 can be used as a low speed FSK demodulator. In this application the center frequency is set to one of the input frequencies, and the bandwidth is adjusted to leave the second frequency outside the detection band. When the input signal is frequency keyed between the *in-band* signal and the *out-band* signal, the logic state of the output at pin 8 is reversed. Figure 26 shows the FSK input ($f_2 = 3\ f_1$) and the demodulated output signals, with $f_o = f_2 = 1$ kHz. The circuit can handle data rates up to $f_o/10$ baud.

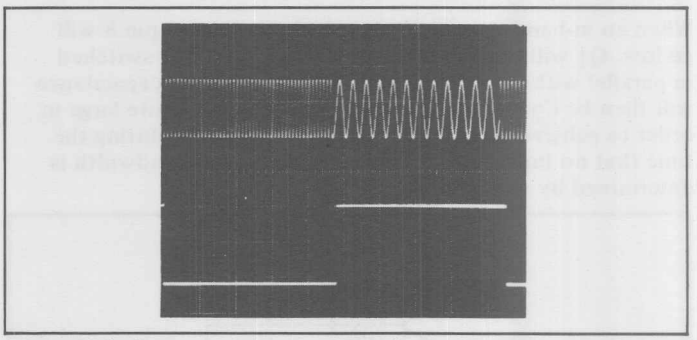


Figure 26. Input and Output Waveforms for FSK Decoding
Top: Input FSK Signal ($f_2 = 3f_1$)
Bottom: Demodulated Output

ORDER INFORMATION

The XR-567 is available in an 8-pin TO-99 metal can and 8-pin, dual-in-line ceramic packages. Package outlines are shown on page 1. Both military and commercial temperature ranges are also available.

Part Number	Package	Temperature Range
XR-567N	dual-in-line	−55°C to +125°C
XR-567CN	dual-in-line	0°C to +75°C
XR-567T	TO-99	−55°C to +125°C
XR-567CT	TO-99	0°C to +70°C

XR-2567

Dual Monolithic Tone Decoder

APRIL 1973

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. Figure 1 is a functional block diagram of the complete monolithic system. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic-compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

FEATURES

Replaces two 567-type decoders
Excellent temperature tracking between decoders
Bandwidth adjustable from 0 to 14%
Logic compatible outputs with 100 mA sink capability
Center frequency matching (1% typ.)
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false triggering
Frequency range adjustable over 20:1 range by external resistor.

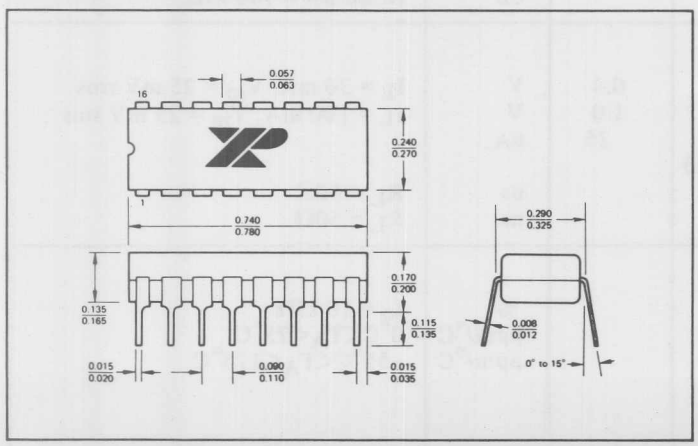
APPLICATIONS

Touch-Tone ® Decoding
Sequential Tone Decoding
Dual-Tone Decoding/Encoding
Communications Paging
Ultrasonic Remote-control and Monitoring
Full-Duplex Carrier-tone Transceiver
Wireless Intercom
Dual Precision Oscillator
FSK Generation and Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	
With Internal Regulator	14V
Without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	750 mW
Derate above +25°C	5 mW/°C
Temperature	
Operating:	
XR–2567	–55°C to +125°C
XR–2567C	0°C to + 75°C
Storage:	–65°C to +150°C

PACKAGE INFORMATION



FUNCTIONAL BLOCK DIAGRAM

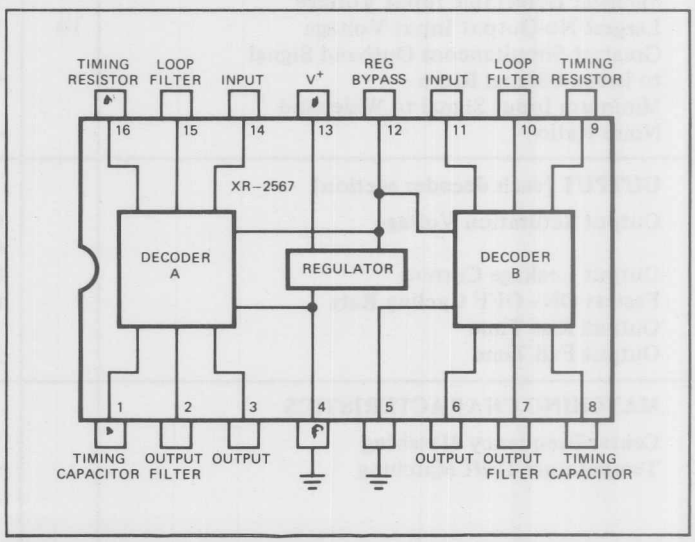


Figure 1. Functional Block Diagram

ELECTRICAL SPECIFICATIONS

Test Conditions: V_{CC} = +5V, T_A = 25°C, unless otherwise specified. Test circuit of Figure 2, S_1 closed unless otherwise specified.

CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range					
Without Regulator	4.75		7	V_{dc}	See Figure 5, S_1 closed.
With Internal Regulator	6.5		12	V_{dc}	See Figure 5, S_1 open.
Supply Current (both decoders)					See Figures 7, 8
Quiescent XR–2567		12	16	mA	R_L = 20 kΩ
XR–2567C		14	20	mA	R_L = 20 kΩ
Activated XR–2567		22	26	mA	R_L = 20 kΩ
XR–2567C		24	30	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			–10	V	
Positive Voltage at Input			V_{CC}+0.5	V	
CENTER FREQUENCY (each decoder section)					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 14
0°<T_A<+75°C		±60		ppm/°C	See Figure 14
–55°<T_A<+125°C		±140		ppm/°C	See Figure 14
Supply Voltage					
Without Regulator					
XR–2567		0.5	1.0	%/V	f_o = 100 kHz
XR–2567C		0.7	2.0	%/V	f_o = 100 kHz
With Internal Regulator					
XR–2567		0.05		%/V	f_o = 100 kHz, V+ = 9V
XR–2567C		0.1		%/V	f_o = 100 kHz, V+ = 9V
DETECTION BANDWIDTH (each decoder section)					
Largest Detection Bandwidth					
XR–2567	12	14	16	% of f_o	f_o = 100 kHz
XR–2567C	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR–2567		1	2	% of f_o	
XR–2567C		1	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
INPUT (each decoder section)					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		–6		dB	Noise Bw = 140 kHz
OUTPUT (each decoder section)					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON–OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω
MATCHING CHARACTERISTICS					
Center Frequency Matching		1		%	f_o = 10 kHz
Temperature Drift Matching		±20		ppm/°C	0°C<T_A<75°C
		±50		ppm/°C	–55°C<T_A<125°C

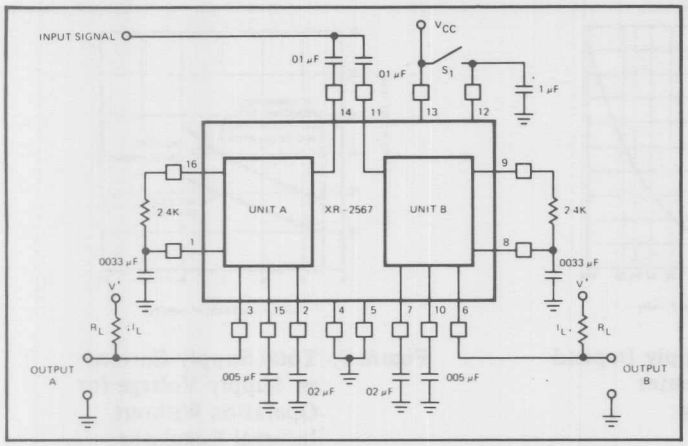
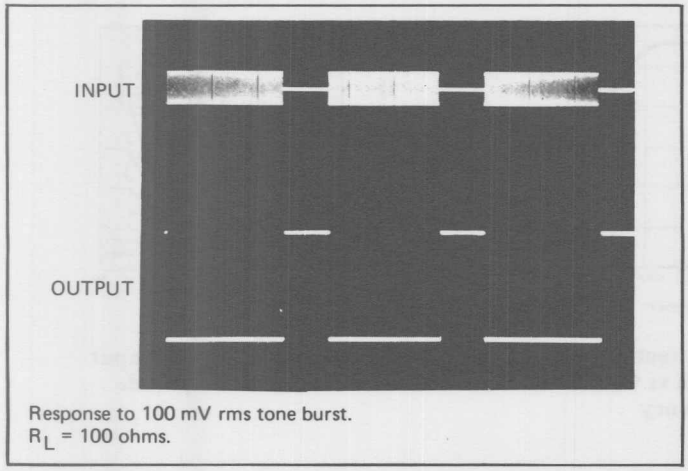


Figure 2. Test Circuit



Response to 100 mV rms tone burst.
R_L = 100 ohms.

Figure 3. XR–2567 Typical Response

DEFINITIONS OF XR–2567 PARAMETERS

f_o is the *free-running frequency* of the current-controlled oscillator of the PLL with no input signal. It is determined by resistor R_1 and capacitor C_1; f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

The *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a "logic zero" state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_o, can be determined by the approximation

$$BW \approx 1070 \sqrt{\frac{V_i}{f_o C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance in μF at pins 10 or 15.

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

DESCRIPTION OF CIRCUIT CONTROLS

INPUT (Pins 11 and 14)

The input signal is applied to pins 14 and/or 11 through a coupling capacitor, C_C. These terminals are internally biased at a dc level 2 volts above ground and they have an input impedance level of approximately 20 kΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 1, 8, 9, and 16)

The center frequency, f_o, of each decoder section is set by a resistor R_1 and a capacitor C_1. R_{1A} is connected between pins 1 and 16 in decoder section A, and R_{1B} between pins 8 and 9 of decoder section B. C_{1A} is connected from pin 1 to ground, and C_{1B} from pin 8 to ground, as shown in Figure 4. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2 k$\Omega \leq R_1 \leq$ 20 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

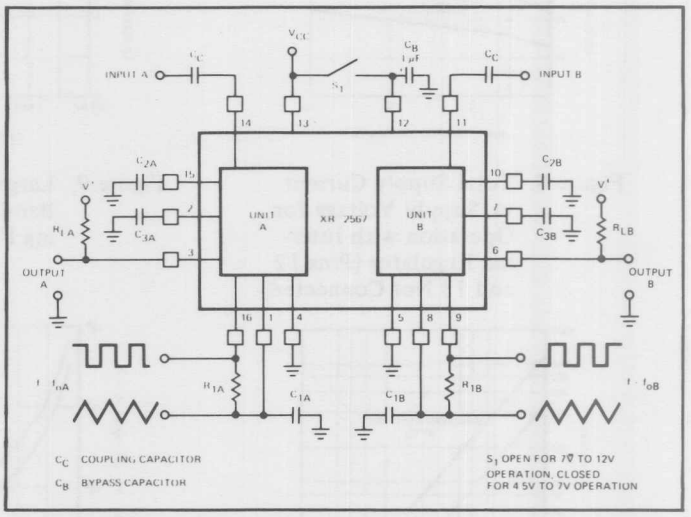


Figure 4. Circuit Connection Diagram

For decoder section A, the oscillator output can be obtained at either pin 1 or 16. Pin 16 is the oscillator squarewave output which has a magnitude of approximately V_{CC}–1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 1 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 1 to avoid disturbing the temperature stability or duty cycle of the oscillator. For section B, pin 9 is the squarewave output and pin 8 the exponential triangle waveform output.

LOOP FILTER, C_2 (Pins 10 and 15)

Capacitors C_{2A} and C_{2B} connected from pins 15 and 10 to ground are the single-pole, low-pass filters for the PLL portion of decoder sections A and B. The filter time constant is given by $T_2 = R_2C_2$, where R_2(10 kΩ) is the impedance at pins 10 or 15. The selection of C_2 is determined by the detection bandwidth requirements and input signal amplitude as shown in Figures 10 and 12. One approach is to select an area of operation from the graph and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires

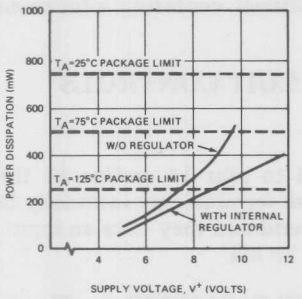


Figure 5. Internal Power Dissipation vs. Supply Voltage. Both Units Activated, R_L = 20 k

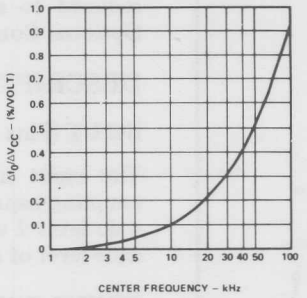


Figure 6. Power Supply Dependence of Center Frequency

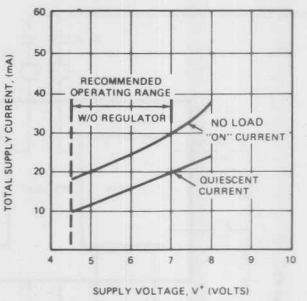


Figure 7. Total Supply Current vs. Supply Voltage for Operation Without Internal Regulator (Pins 12 and 13 Shorted)

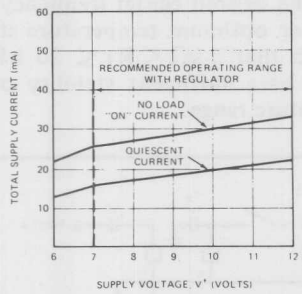


Figure 8. Total Supply Current vs. Supply Voltage for Operation with Internal Regulator (Pins 12 and 13 Not Connected)

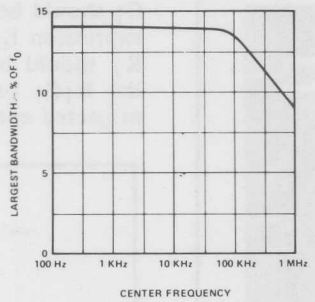


Figure 9. Largest Detection Bandwidth vs Operating Frequency

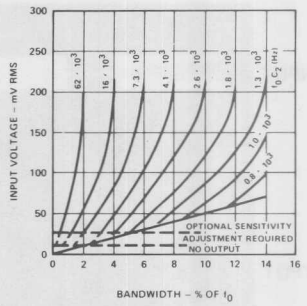


Figure 10. Bandwidth vs Input Signal Amplitude

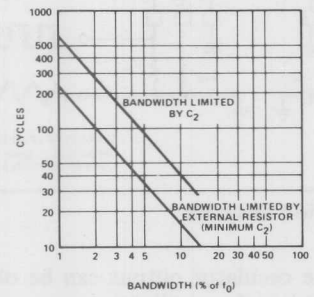


Figure 11. Greatest Number of Cycles Before Output

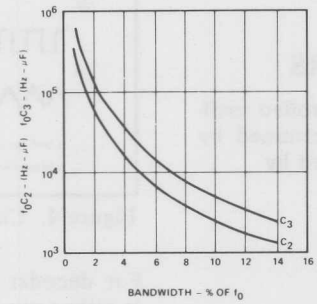


Figure 12. Detection Bandwidth as a Function of C_2 and C_3

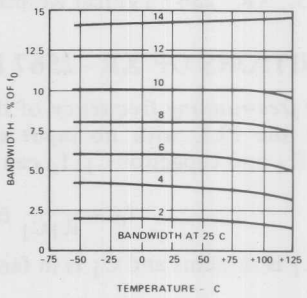


Figure 13. Bandwidth Variation With Temperature

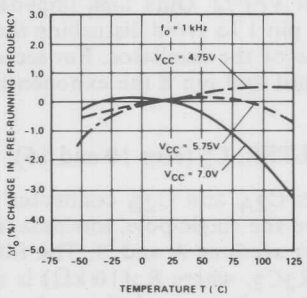


Figure 14. Frequency Drift With Temperature

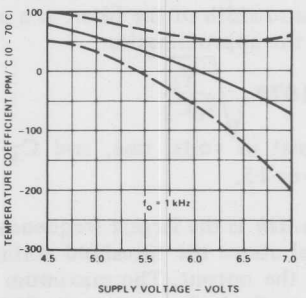


Figure 15. Temperature Coefficient of Center Frequency (Mean and S.D.)

$V_i > 200$ mV rms. Then, as noted in Figure 10, bandwidth will be controlled solely by the f_oC_2 product. (For additional information, see Optional Controls Section, "Speed of Response" and "Bandwidth Reduction".)

Pins 10 and 15 correspond to the PLL phase detector outputs of sections A and B, respectively. The voltage level at these pins is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

OUTPUT FILTER, C_3 (Pins 2 and 7)

Capacitors C_{3A} and C_{3B} connected from pins 2 and 7 to ground form low-pass post detection filters for sections A and B respectively. The function of the post detection filter is to eliminate spurious outputs caused by out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3(4.7 k) is the internal impedance at pins 2 or 7.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, a minimum value for C_3 is $2C_2$, where C_2 is the loop filter capacitance for the corresponding decoder section. If C_3 is smaller than $2C_2$, then frequencies adjacent to the detection band may switch the output stage "off" and "on" at the beat frequency, or the output may pulse "off" and "on" during the turn-on transient.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, this delay may be desirable as a means of suppressing spurious outputs. (For additional information, see Optional Controls Section, "Speed of Response" and "Chatter".)

LOGIC OUTPUT (Pins 3 and 6)

Output terminals 3 and 6 provide a binary logic output when an input signal tone is present within the detection-band of each respective decoder section. The logic outputs are uncommitted "bare-collector" power transistors capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from V_{CC} to pins 3 or 6.

When an in-band signal is present, the output transistor at pins 3 or 6 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+ higher than the V_{CC} supply. For safe operation, V+ $\leq$ 15 volts.

REGULATOR BY-PASS (Pin 12)

This pin corresponds to the output of the voltage regulator section. For circuit operation with a supply voltage greater than 7V, pin 12 should be ac grounded with a bypass capacitor $\geq 1\ \mu$F. For circuit operation over a supply voltage range of 4.5 to 7V, the voltage regulator section is not required; pin 12 should be shorted to V_{CC}.

GROUND TERMINALS (Pins 4 and 5)

To eliminate parasitic interaction, each decoder section has a separate ground terminal. The internal regulator shares a common ground with decoder section A (pin 4).

Independent ground terminals also allow additional flexibility for split supply operation. Pin 4 can be used as V−, and pin 5 as ground, as shown in Figure 16. When the circuit is operated with split supplies, the positive supply should always be > 6V, and the dc potential across pins 13 and 4 should not exceed 15 volts.

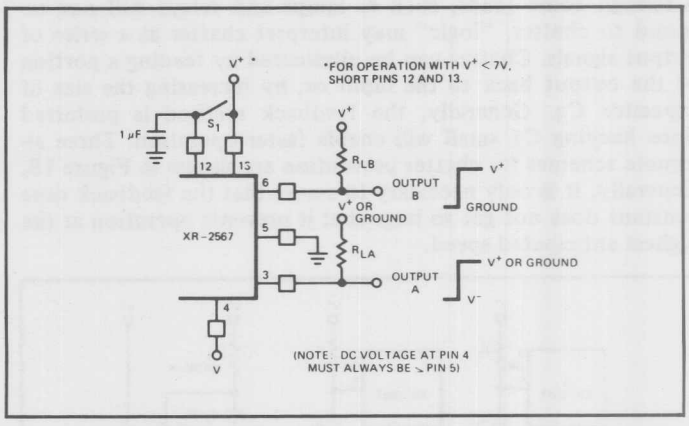


Figure 16. Split-Supply Operation Using Independent Ground Terminals of Units A and B. Unit A Operates Between V^+ and V^-; Unit B Operates Between V^+ and Ground

OPTIONAL CONTROLS

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus, maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}, \quad C_3 = \frac{260}{f_o}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 17 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

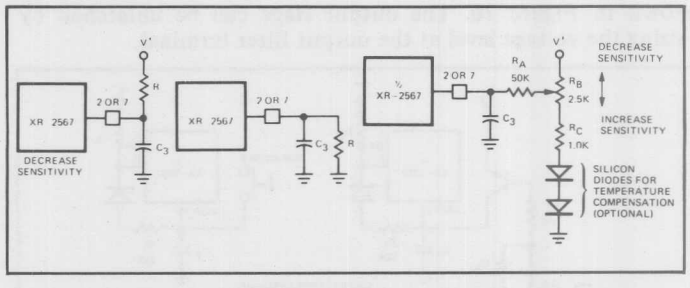


Figure 17. Optional Connections for Sensitivity Control

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, "logic" may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 18. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

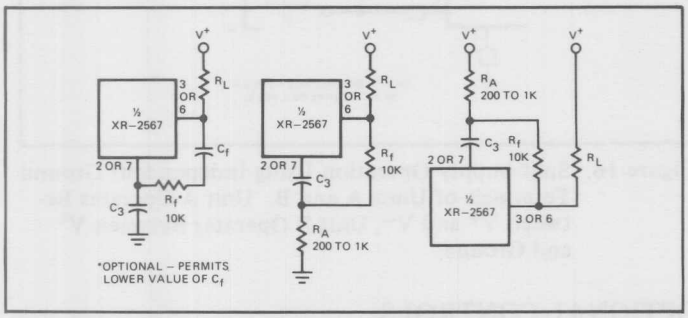


Figure 18. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Figure 19 can be used to change the position of the detection band (capture range) within the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

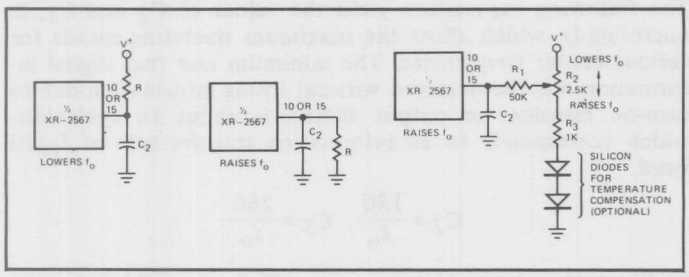


Figure 19. Connections to Reposition Detection Band

OUTPUT LATCHING

After a signal is received, the output of either decoder section can be latched "on" by connecting a 20 kΩ resistor and diode from the "output" terminal to the "output filter" terminal as shown in Figure 20. The output stage can be unlatched by raising the voltage level at the output filter terminal.

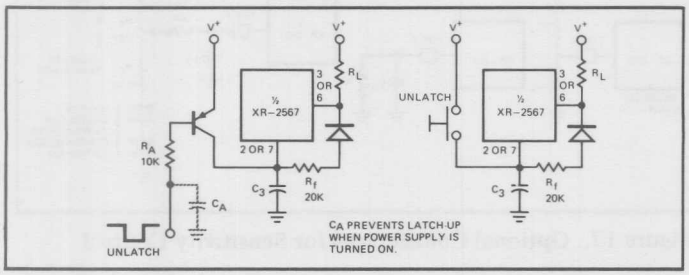


Figure 20. Output Latching

POSITIONING OF DETECTION BANDS

Figure 21 defines the respective band-edge and band-center frequencies for sections A and B of the dual tone decoder. Frequencies f_L and f_H with appropriate subscripts refer to the low and the high band-edge frequencies for decoder sections A and B, and f_o is the center frequency.

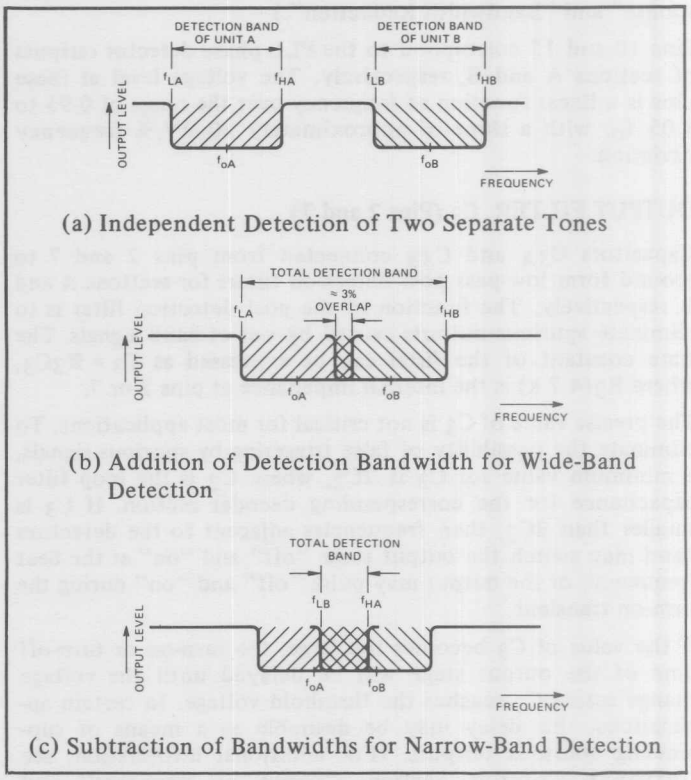


Figure 21. Positioning of Detection Bands

The two sections can be interconnected to form a single tone detector with an overall detection bandwidth equal to the sum or the difference of the detection bands for the two individual detector sections. For example, if the individual decoder sections are interconnected as shown in Figure 25, then the total detection bandwidth would be approximately equal to the sum of the respective bandwidths as shown in Figure 21(b). Similarly, if the decoders are interconnected as shown in Figure 23, then the overall detection band would be equal to the difference, or the overlap, between the respective bandwidths as shown in Figure 21(c).

BANDWIDTH REDUCTION

The bandwidth of each decoder can be reduced by either increasing the loop filter capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 22 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation.

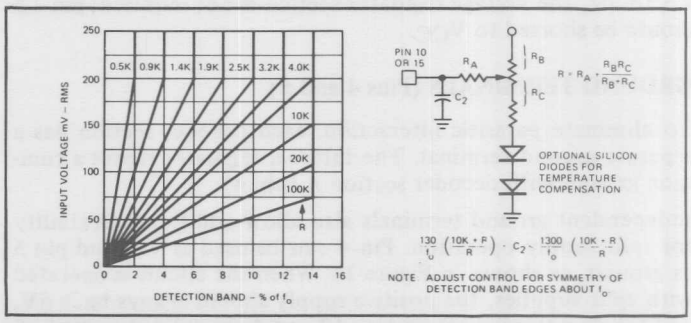


Figure 22. Bandwidth Reduction

Bandwidth reduction can also be obtained by subtracting overlapping bandwidths of the two decoder sections (see Figures 21(c) and 23).

APPLICATIONS

DUAL-TONE DETECTION

In most dual-tone detection systems, the decoder output is required to change state only when *both* input tones are present simultaneously. This can be implemented by setting the detection bandwidth of each of the XR−2567 decoder sections to cover one of the input tones; and then connecting the respective outputs through a NOR gate, as shown in Figure 23. In this case, the output of the NOR gate will be "high" only when both input tones are present simultaneously.

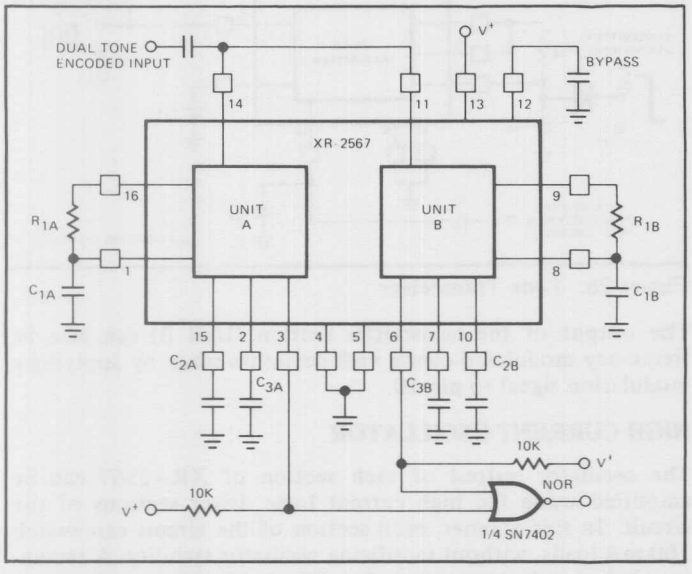


Figure 23. Connection for Decoding Dual-Tone Encoded Input Signals

Figure 24 shows additional circuit configurations which can be used for decoding multiple-tone input signals. In Figure 24(a), the output of Unit A is connected to the output filter (pin 7) of Unit B through the diode D_1. *If no input tone is present within the detection-band of Unit A,* then its output (pin 3) is "high", which keeps diode D_1 conducting and "disables" Unit B by keeping its output (pin 6) "high". *If an input tone is present within the detection-band of Unit A,* pin 3 is low, diode D_1 is reverse biased, and decoder B is no longer disabled. If under these conditions an input signal is present within the detection-band of Unit B, then its output at pin 6 would be "low". Thus, the output at pin 6 is "low" only when input tones within the detection-band of A and B are present simultaneously.

The dual-tone decoder circuit of Figure 24(b) makes use of the split-ground feature of the XR−2567. The output terminal of Unit A is used as a "switch" in series with the ground terminal (pin 5) of Unit B. If the input tone A is not present, pin 3 is at its high-impedance state, and the ground terminal of Unit B is open-circuited. When the input tone A is present, pin 3 goes to a low-impedance state and Unit B is activated. In this manner, the output of Unit B will be "low" *only* when both tones A and B are present.

In the circuit connection of Figure 24(b), Unit B does not draw any current until it is activated. Therefore, its power dissipation in a stand-by condition is lower than other dual-tone decoder configurations. However, due to finite series resistance between pin 3 and ground when Unit B is activated, the output current sink capability is limited to ≤ 10 mA.

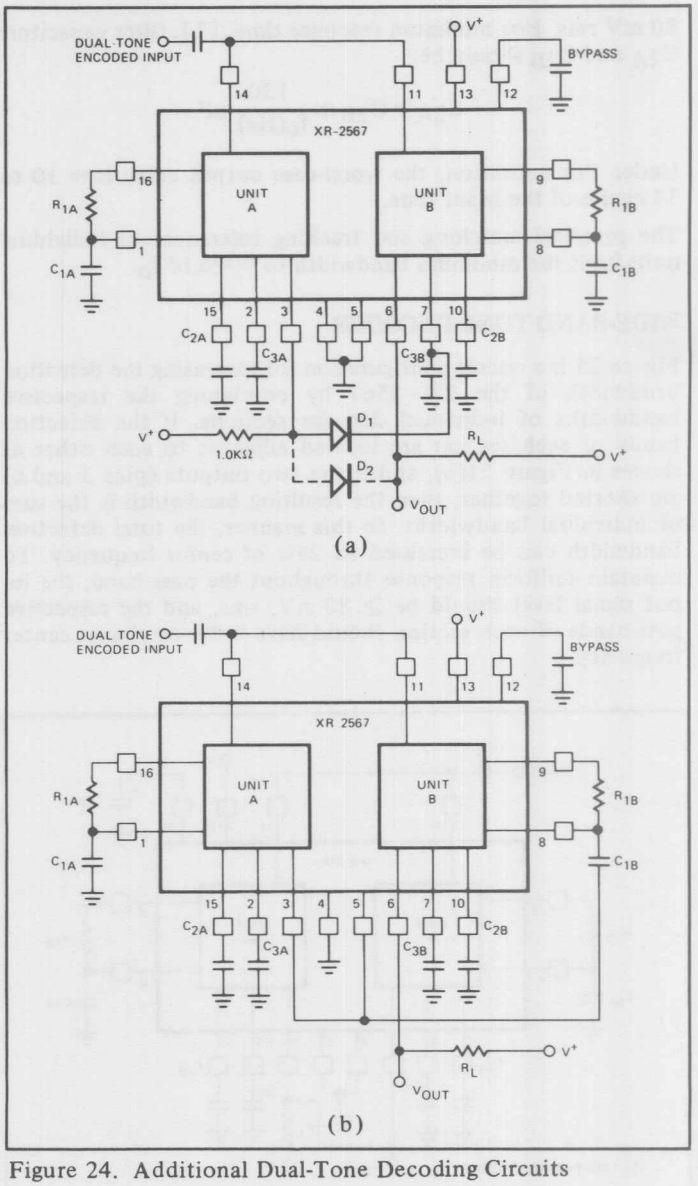


Figure 24. Additional Dual-Tone Decoding Circuits

SEQUENTIAL TONE DECODING

Dual-tone decoder circuits can also be used for sequential tone decoding where one tone must be present before the other for the circuit to operate. This can be achieved by making the output filter capacitance, C_3, of one of the sections large with respect to the other. For example, in the circuits of Figures 24(a) and 24(b), if C_{3A} is chosen to be much larger than C_{3B} ($C_{3A} \geq C_{3B}$), then Unit A will remain "on" and activate B for a finite time duration after tone A is terminated. Thus, the circuit will be able to detect the two tones only if they are present sequentially, with tone A preceding tone B.

The circuit of Figure 24(a) can also be modified for sequential tone decoding by addition of a diode, D_2, between pins 3 and 6. Once activated by Unit A, Unit B will stay "on" as long as tone B is present, even though tone A may terminate. Once tone B disappears, the circuit is reset to its original state and would require tone A to be present for activation.

HIGH-SPEED NARROW-BAND TONE DECODER

The circuit of Figure 23 can be used as a narrow-band tone decoder by overlapping the detection bands of Units A and B (see Figure 21(c)). The output of the NOR gate will be high only when an input signal is present within the overlapping portions of the detection band. To maintain uniform response within the pass-band, the input signal amplitude should be $\geq$

80 mV rms. For minimum response time, PLL filter capacitors C_{2A} and C_{2B} should be:

$$C_{2A} = C_{2B} \cong \frac{130}{f_o(Hz)}\ \mu F$$

Under this condition, the worst-case output delay is ≈ 10 to 14 cycles of the input tone.

The practical matching and tracking tolerances of individual units limit the minimum bandwidth to ≈ 4% of f_o.

WIDE-BAND TONE DECODER

Figure 25 is a circuit configuration for increasing the detection bandwidth of the XR–2567 by combining the respective bandwidths of individual decoder sections. If the detection bands of each section are located adjacent to each other as shown in Figure 21(b), and if the two outputs (pins 3 and 6) are shorted together, then the resulting bandwidth is the sum of individual bandwidths. In this manner, the total detection bandwidth can be increased to 24% of center frequency. To maintain uniform response throughout the pass band, the input signal level should be ≥ 80 mV, rms, and the respective pass-bands of each section should have ≈ 3% overlap at center frequency.

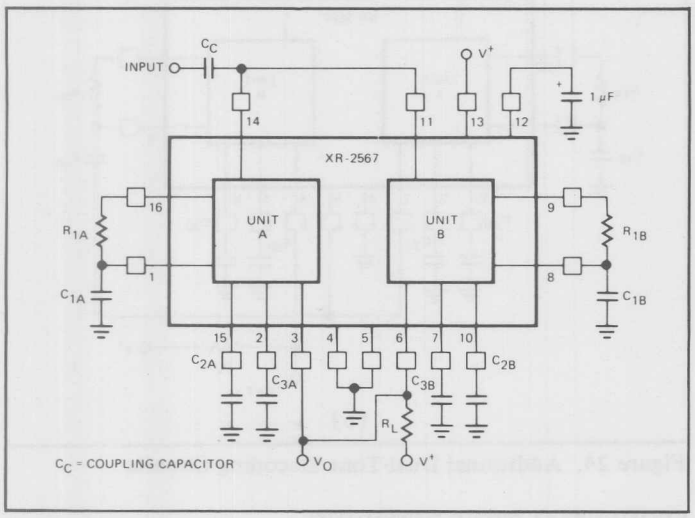


Figure 25. Wide-Band Tone Detection

TONE TRANSCEIVER

The XR–2567 can be used as a full-duplex tone transceiver by using one section of the unit as a tone detector and the remaining section as a tone generator. Since both sections operate independently, the circuit can transmit and receive simultaneously. A recommended circuit connection for transceiver applications is shown in Figure 26. In this case, Unit A is utilized as the receiver, and Unit B is used as the transmitter.

The transmitter section can be keyed "on" and "off" by applying a pulse to pin 8 through a disconnect diode D_1. The oscillator section of Unit B will be keyed "off" when the keying logic level at pin 8 is at a "low" state.

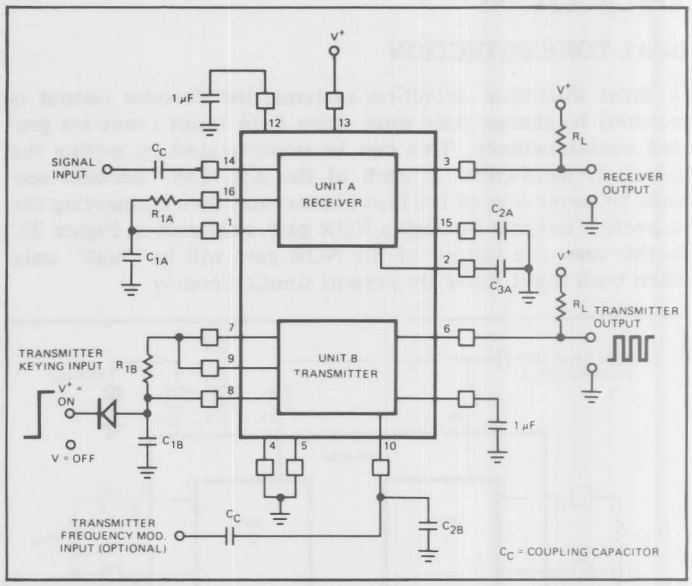


Figure 26. Tone Transceiver

The output of the transmitter section (Unit B) can also be frequency modulated over a +6% deviation range by applying a modulation signal to pin 10.

HIGH CURRENT OSCILLATOR

The oscillator output of each section of XR–2567 can be amplified using the high current logic driver sections of the circuit. In this manner, each section of the circuit can switch 100 mA loads, without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 27. The oscillator frequency can be modulated over ±6% of f_o by applying a control voltage to pins 15 or 10.

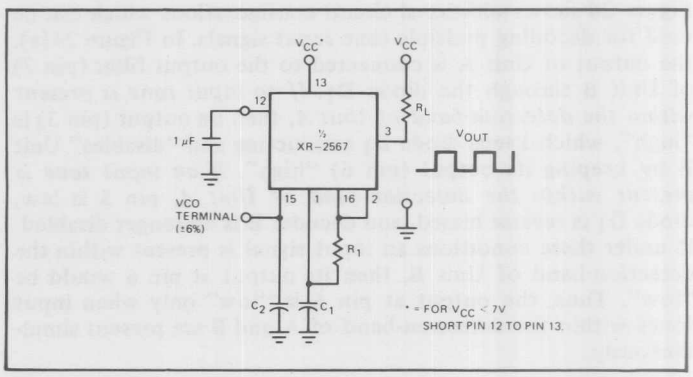


Figure 27. Precision Oscillator with High Current Output Capability

Application Note AN-01

Stable FSK Modems Featuring the XR-2207, XR-2206 and XR-2211

October 1976

INTRODUCTION

Frequency shift keying (FSK) is the most commonly-used method for transmitting digital data over telecommunications links. In order to use FSK, a modulator-demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again.

This Applications Note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application.

The devices featured in this Application Note are the XR-2206 and XR-2207 FSK modulators, and the XR-2211 FSK demodulator with carrier-detect capability. Because of the superior frequency stability (typically 20 ppm/°C) of these devices, a properly designed modem using them will be virtually free of the temperature and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60 dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modem designs shown in this Applications Note can be used with mark and space frequencies anywhere from several Hertz to 100 kiloHertz.

THE XR-2206 FSK MODULATOR

FEATURES

- Typically 20 ppm/°C temperature stability
- Choice of 0.5% THD sinewave, triangle, or squarewave output
- Phase-continuous FSK output
- Inputs are TTL and C/MOS compatible
- Low power supply sensitivity (0.01%/V)
- Split or single supply operation
- Low external parts count

OPERATION

The XR-2206 is ideal for FSK applications requiring the spectral purity of a sinusoidal output waveform. It offers TTL and C/MOS compatibility, excellent frequency stability, and ease of application. The XR-2206 can typically provide a 3 volt p-p sinewave output. Total harmonic distortion can be trimmed to 0.5%. If left untrimmed, it is approximately 2.5%.

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to pin 9. A high level signal selects the frequency $(1/R_6C_3)$ Hz; a low level signal selects the frequency $(1/R_7C_3)$ Hz, (resistors in ohms and capacitors in farads). For optimum stability, R_6 and R_7 should be within the range of 10 kΩ to 100 kΩ. The voltage applied to pin 9 should be selected to fall between ground and V+.

Note: Over and under voltage may damage the device.

Potentiometers R_8 and R_9 should be adjusted for minimum total harmonic distortion. In applications where minimal distortion is unnecessary, pins 15 and 16 may be left open-circuited and R_8 may be replaced by a fixed 200Ω resistor. In applications where a triangular output waveform is satisfactory, pins 13 thru 16 may be left open-circuited.

The output impedance at pin 2 is about 600Ω with AC coupling normally be used.

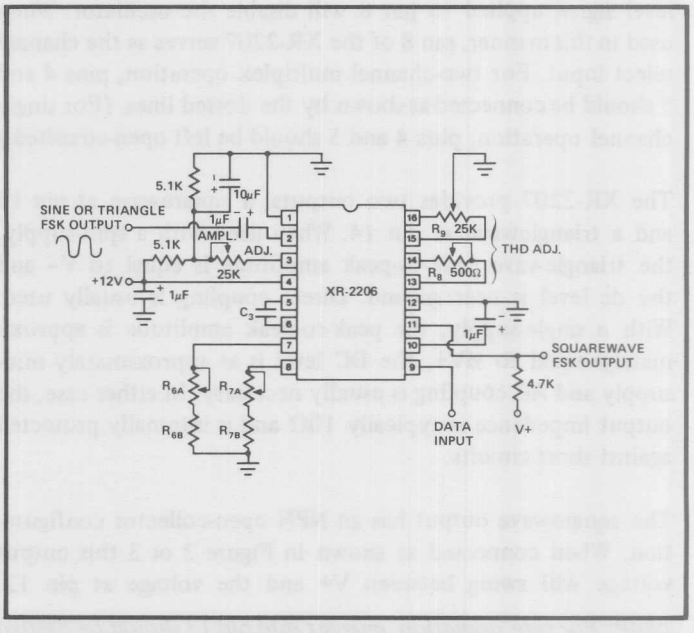


Figure 1. The XR-2206 Sinusoidal FSK Generator

THE XR-2207 FSK MODULATOR

FEATURES

- Typically 20 ppm/°C temperature stability
- Phase-continuous FSK output
- Provides both triangle and squarewave outputs
- Operates single-channel or two-channel multiplex
- Inputs are TTL and C/MOS compatible
- Split or single power supply operation
- Low power supply sensitivity (0.15%/V)
- Low external parts count

OPERATION

The XR-2207 is a stable FSK generator which is designed for those applications where only a triangle or squarewave output is required. It is capable of either single-channel or two-channel multiplex operation, and can be used easily with either split or single power supplies.

Figure 2 shows the XR-2207 using a single-supply and Figure 3 shows split-supply operation. When used as an FSK modulator pins 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and C/MOS logic forms. When used with a single supply, the threshold is near mid-supply and is C/MOS compatible. Table 1 shows how to select the timing resistors R_1 thru R_4 to determine the output frequency based upon the logic levels applied to pins 8 and 9. For optimum stability, the values of R_1 and R_3 should be selected to fall between 10 kΩ and 100 kΩ.

With pin 8 grounded, pin 9 serves as the data input. A high level signal applied to pin 8 will disable the oscillator. When used in this manner, pin 8 of the XR-2207 serves as the channel select input. For two-channel multiplex operation, pins 4 and 5 should be connected as shown by the dotted lines. (For single channel operation, pins 4 and 5 should be left open-circuited.)

The XR-2207 provides two outputs; a squarewave at pin 13 and a trianglewave at pin 14. When used with a split-supply, the trianglewave peak-to-peak amplitude is equal to V– and the dc level is near ground. Direct coupling is usually used. With a single-supply, the peak-to-peak amplitude is approximately equal to ½V+, the DC level is at approximately mid-supply and AC coupling is usually necessary. In either case, the output impedance is typically 10Ω and is internally protected against short circuits.

The squarewave output has an NPN open-collector configuration. When connected as shown in Figure 2 or 3 this output voltage will swing between V+ and the voltage at pin 12.

Note: For safe operation, current into pin 13 should be limited to 20 mA.

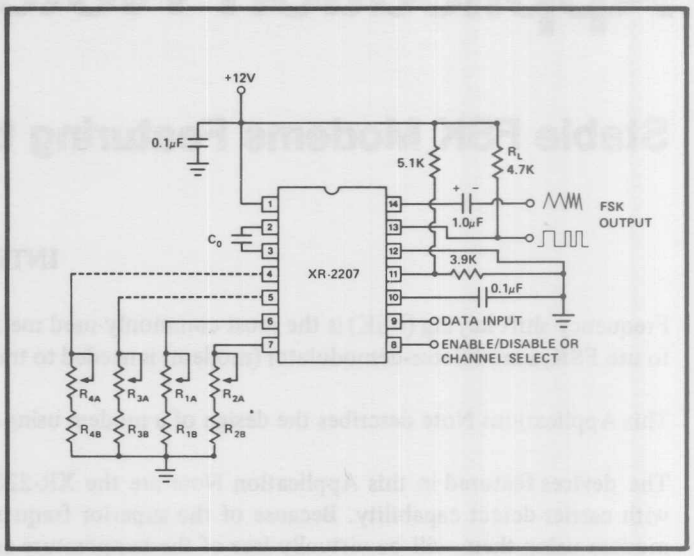


Figure 2. The XR-2207 FSK Modulator Single-Supply Operation

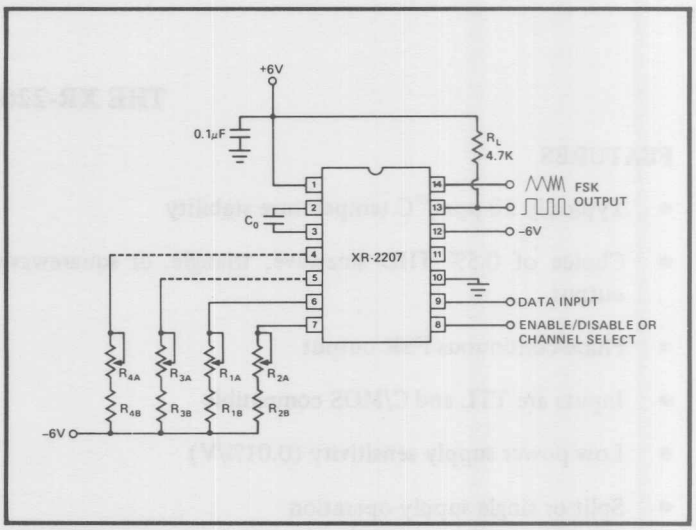


Figure 3. The XR-2207 FSK Modulator Split-Supply Operation

TABLE 1
XR-2207 FSK Input Control Logic

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pins 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

Units: Resistors – Ohms; Capacitors – Farads; Frequency – Hz

THE XR-2211 FSK DEMODULATOR WITH CARRIER DETECT

FEATURES

- Typically 20 ppm/°C temperature stability
- Simultaneous FSK and carrier-detect output
- Outputs are TTL and C/MOS compatible
- Wide dynamic range (2 mV to 3 Vrms)
- Split or single supply operation
- Low power supply sensitivity (0.05%/V)
- Low external parts count

OPERATION

The XR-2211 is a FSK demodulator which operates on the phase-locked-loop principle. Its performance is virtually independent of input signal strength variations over the range of 2 mV to 3 Vrms.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. F_0 should be calculated to fall midway between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula: $\Delta f = (R_4 f_0/R_5)$ Hz. Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an R_4 between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_c$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop filter time constant. In most modem applications, $\Delta f_c = (80\% - 99\%)\ \Delta f$.

The loop damping factor (ζ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. It is determined by $\zeta = \frac{1}{4}\sqrt{C_1/C_2}$. For most modem applications, choose $\zeta \approx \frac{1}{2}$.

The FSK output filter time constant (τ_F) removes chatter from the FSK output. The formula is: $\tau_F = R_F C_F$. Normally calculate τ_F to be approximately equal to [0.3/(baud rate)] seconds.

The lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: $C_D\ (\mu f) \approx 16$/capture range in Hz.

Note: Excessive values of C_D will unnecessarily slow the lock-detect response time.

The XR-2211 has three NPN open collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output, which goes low when a carrier is detected, and Pin 6 is the $\overline{Q}$ lock detect output, which goes high when lock is detected. If pins 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied and will be "low" when no carrier is present.

If the lock-detect feature is not required, pins 3, 5 and 6 may be left open-circuited.

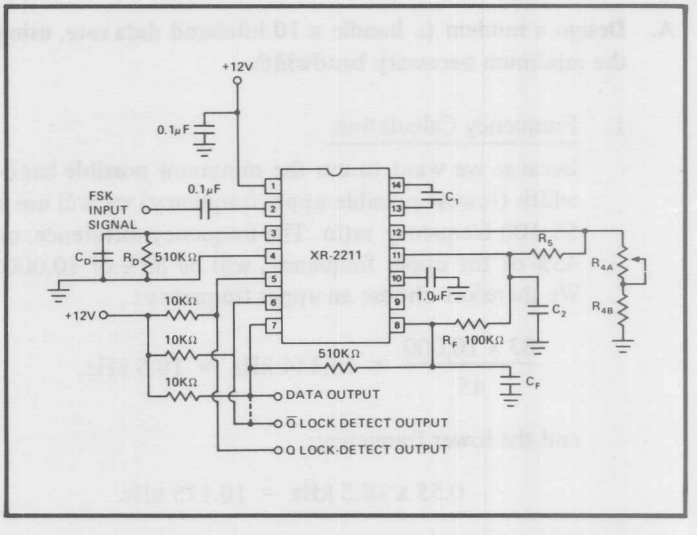


Figure 4. The XR-2211 FSK Demodulator with Carrier Detect

DESIGNING THE MODEM

Table 2 shows recommended component values for the three most commonly used FSK bands. In many instances, system constraints dictate the use of some non-standard FSK band. The XR-2206/XR-2207, XR-2211 combination is suitable for any range of frequencies from several Hertz to 100 kiloHertz.

Here are several guidelines to use when calculating non-standard frequencies:

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55% of the upper frequency. (Less than a 2:1 ratio)
- For minimum demodulated output pulsewidth jitter, select an FSK band whose mark and space frequencies are

both high compared to the baud rate. (i.e., for a 300 baud channel, mark and space frequencies of 2025 Hz and 2225 Hz would result in significantly less pulsewidth jitter than 300 Hz and 550 Hz).

- For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship

$$\frac{\text{mark-space frequency difference (Hz)}}{\text{maximum data rate (baud)}} \geqslant 83\%$$

should be observed.

For narrower spacing, the minimum ratio should be about 67%.

- The values shown in Table 2 may be scaled proportionately for mark and space frequencies, maximum baud rate, and (inversely) capacitor value. It is best to retain (approximately) the resistor values shown.

TABLE 2
Recommended Component Values for Typical FSK Bands

FSK Band			XR-2207					XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{1A} R_{3A}	R_{1B} R_{3B}	R_{2A} R_{4A}	R_{2B} R_{4B}	C_0	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_{4A}	R_{4B}	R_5	C_1	C_2	C_F	C_D
300	1070	1270	10	20	100	100	.039	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
300	2025	2225	10	18	150	160	.022	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05
1200	1200	2200	20	30	20	36	.022	10	16	20	30	.022	10	18	30	.027	.01	.0022	.01

Units: Frequency – Hz; Resistors – kΩ; Capacitors – μF

DESIGN EXAMPLES

A. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.

1. Frequency Calculation

Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore choose an upper frequency:

$$\frac{83 \times 10{,}000}{45} = 18.444 \text{ kHz} \approx 18.5 \text{ kHz}.$$

and the lower frequency:

$$0.55 \times 18.5 \text{ kHz} = 10.175 \text{ kHz}.$$

2. Component Selection

a. For the XR-2207 FSK modulator, set $R_1 \approx 30\,k\Omega$. Now, select a value of C_0 to generate 10.175 kHz with R_1:

$$10.175 \text{ kHz} = 1/(C_0 \times 30{,}000)\ ;\ C_0 = 3300 \text{ pF}.$$

To choose R_2:

$$18.500 \text{ kHz} - 10.175 \text{ kHz} = 8.325 \text{ kHz} = 1/C_0R_2\ ;\ R_2 = 36\,k\Omega.$$

A good choice would be to use 10 kΩ potentiometers for R_{1A} and R_{2A}, and to set $R_{1B} = 24\,k\Omega$ and $R_{2B} = 30\,k\Omega$.

b. For the XR-2206, we can make R_7 equal to R_1 and C_3 equal to C_0 above. To determine R_6:

$$18.5 \text{ kHz} = 1/R_6C_3\ ;\ R_6 = 16\,k\Omega.$$

Use a 10 kΩ potentiometer for R_{6A} and set $R_{6B} = 13\,k\Omega$.

c. For the XR-2211 demodulator, we need to first determine R_4 and C_1. First, $f_0 = (f_L + f_H)/2 = (10.175 + 18.500)/2 = 14.338$ kHz. If we make $R_4 = 25\,k\Omega$, then $1/(C_1 \times 25{,}000) = 14{,}338$; $C_1 = 2790\,pF \approx 2700$ pF. With that value of C_1, the precise value of R_4 is now 25.8 kΩ. Select $R_{4B} = 18\,k\Omega$ and use a 10 kΩ for R_{4A}.

3. Frequency Component Selection

a. To calculate R_5, we first need our Δf, which is 18.500 – 10.175, or 8.325 kHz.

$$8325 = (25{,}800 \times 14{,}338)/R_5\ ;\ R_5 = 44.4\,k\Omega \approx 47\,k\Omega.$$

b. To determine C_2 use $\zeta = \frac{1}{2} = \frac{1}{4}\sqrt{C_1/C_2}$. Then, $C_2 = \frac{1}{4}C_1$; $C_2 = 670$ pF.

c. To select C_F, we use τ_F = [0.3/(baud rate)] seconds.

$$\tau_F = 0.3/10{,}000 = 30\ \mu\text{sec.}\ ;$$

with

$$R_F = 100\,k\Omega,\ C_F = 300 \text{ pF}.$$

4. Lock Range Selection

To select C_D, let us start with the actual lock range:

$$\Delta f = R_4 f_0 / R_5 \text{ Hz} = 7870 \text{ Hz}.$$

If we assume a capture range of 80%,

$$\Delta f_C = 6296 \text{ Hz};$$

therefore, our total capture range or $\pm\Delta f_C$ is 12,592 Hz. Our minimum value for C_D is (16/12,592) μf or 0.0013 μf.

5. Completed Circuit Example

See Figure 5.

B. Design a 3 kilobaud modem to operate with low output jitter. The bandwidth available is 13 kHz.

For this modem, we can take the values from 2 for the 300 baud modem operating at 1070 Hz and 1270 Hz, multiply our baud rate and mark and space frequencies by 10, and divide all capacitor values on the table by 10. Resistor values should be left as they are.

C. Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600 Hz and 900 Hz, and 1400 and 1700 Hz. (Each of these channels could handle about 400 baud.)

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between 10 kΩ and 100 kΩ: R_1, R_1/R_2, R_3 and R_3/R_4. The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about 20 kΩ, we have: $1700 = 1/(C_0 \times 20{,}000)$; $C_0 = 0.029$ μf which is approximately equal to 0.033 μf.

Calculating R_1 using 600 Hz and 0.033 μf, we get R_1 = 50.5 kΩ. We can use R_{1B} = 47 kΩ and R_{1A} = 10 kΩ. For R_2, we get 101 kΩ. Use R_{2B} = 91 kΩ and R_{2A} = 20 kΩ. To determine R_3, use: 1400 Hz = $1/R_3C_0$, which gives us R_3 = 21.6 kΩ. Use R_{3B} = 18 kΩ and R_{3A} = 5 kΩ. R_4 must generate a 300 Hz shift in frequency, the same as R_2. Therefore set R_4 equal to R_2.

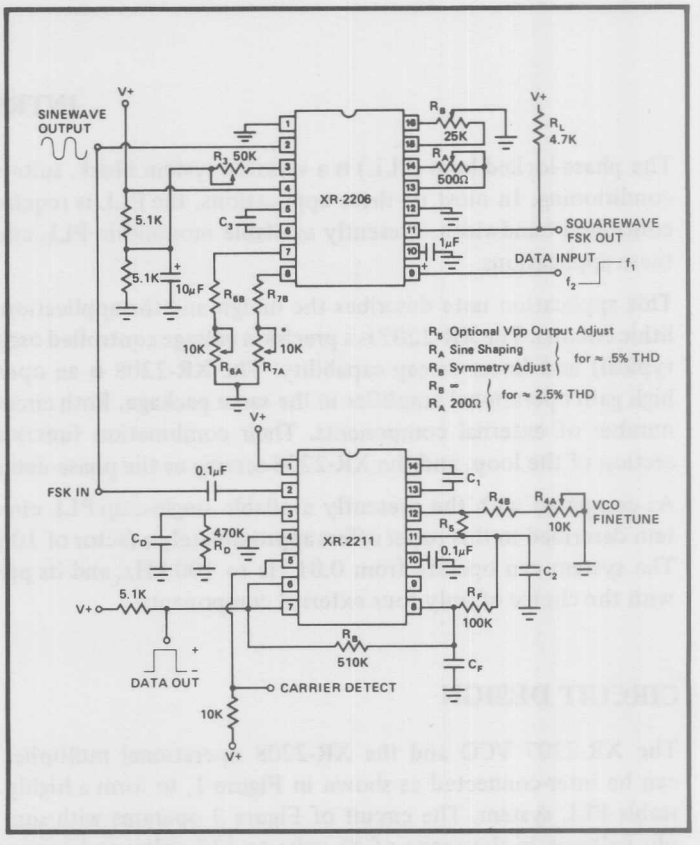


Figure 5. Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values.)

ADJUSTMENT PROCEDURE

The only adjustments that are required with any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

The XR-2207: Always adjust the lower frequency first with R_{1B} or R_{3B} and a low level on pin 9. Then with a high level on pin 9, adjust the high frequency using R_{2B} or R_{4B}. The second adjustment affects only the high frequency, whereas the first adjustment affects both the low and the high frequencies.

The XR-2206: The upper and lower frequency adjustments are independent so the sequence is not important.

The XR-2211: With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_0 can be monitored:

1. Short pin 2 to pin 10 and measure f_0 at pin 3 with C_D disconnected;
2. Open R_5 and monitor pin 13 or 14 with a high-impedance probe; or
3. Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

Note: Do* NOT *adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

For further information regarding the use of the XR-2207, XR-2206 and XR-2211 refer to the individual product data sheets.

Application Note AN-06

Precision PLL System Using the XR-2207 and the XR-2208

APRIL 1978

INTRODUCTION

The phase-locked loop (PLL) is a versatile system block, suitable for a wide range of applications in data communications and signal conditioning. In most of these applications, the PLL is required to have a highly stable and predictable center frequency and a well controlled bandwidth. Presently available monolithic PLL circuits often lack the frequency stability and the versatility required in these applications.

This application note describes the design and the application of two-chip PLL system using the XR-2207 and the XR-2208 monolithic circuits. The XR-2207 is a precision voltage controlled oscillator (VCO) circuit with excellent temperature stability (±20 ppm/°C, typical) and linear sweep capability. The XR-2208 is an operational multiplier which combines a four quadrant multiplier and a high gain operational amplifier in the same package. Both circuits are designed to interface directly with each other with a minimum number of external components. Their combination functions as a high performance PLL, with the XR-2207 forming the VCO section of the loop, and the XR-2208 serving as the phase-detector and loop amplifier.

As compared with the presently available single-chip PLL circuits such as the XR-210 or the Harris HI-2820, the two-chip PLL system described in this paper offers approximately a factor of 10 improvement in temperature stability and center frequency accuracy. The system can operate from 0.01 Hz to 100 kHz, and its performance characteristics can be tailored to given design requirements with the choice of only four external components.

CIRCUIT DESIGN

The XR-2207 VCO and the XR-2208 operational multiplier can be inter-connected as shown in Figure 1, to form a highly stable PLL system. The circuit of Figure 3 operates with supply voltages in the range of ±6 volts to ±13 volts; and over a frequency range of 0.01 Hz to 100 kHz. In the PLL system of Figure 3, all the basic performance characteristics of the PLL can be controlled and adjusted by the choice external 4 components identified as resistors R_0 and R_1, and the capacitors C_0 and C_1, C_0 and R_0 control the VCO center frequency; R_1 and C_1 determine the tracking range and the low pass filter characteristics. The two-chip PLL system can be readily converted to single supply operation by inter-connecting the circuit as shown in Figure 2. The PLL circuit of Figure 2 operates over a supply voltage range of +12V to +26V.

For best results, the timing resistor R_0 should be in the range of 5k to 100k, and $R_1 > R_0$. Under these conditions, the basic parameters of the PLL can be easily calculated from the design equations listed in Table 1.

Compared to single-chip PLL circuits, the two-chip precision PLL system shown in Figures 1 and 2 has the following added versatility: each and every key parameter of the system performance can be externally adjusted or tailored to meet a specific requirement, by use of the design equations given in Table 1. This is because each of the key system nodes, i.e. the phase-detector and the VCO inputs and outputs are externally accessible.

Design Example

As an example, consider the design of a PLL system using the circuit of Figure 1, to meet the following nominal performance specifications:

a) Center Frequency = 10 kHz
b) Tracking Range = 20% (9 kHz to 11 kHz)
c) Capture Range = 10% (9.5 kHz to 10.5 kHz)

Solution:

a) Set Center Frequency:
Choose R_0 = 10k (Arbitrary choice for $5k < R_0 < 100k$)
Then, from equation 1 of Table 1:
$C_0 = (1/f_0 R_0) = 0.01\ \mu F$

b) Set Lock Range:
From equation 2 of Table 1:
$R_1 = (0.45)\ R_0 = 45k$

c) Set Capture Range:
Since capture range is significantly smaller than Lock range, equation 8(a) applies.
Solving equation 8(a) for C_1, one obtains:
$C_1 = 0.032\ \mu F$

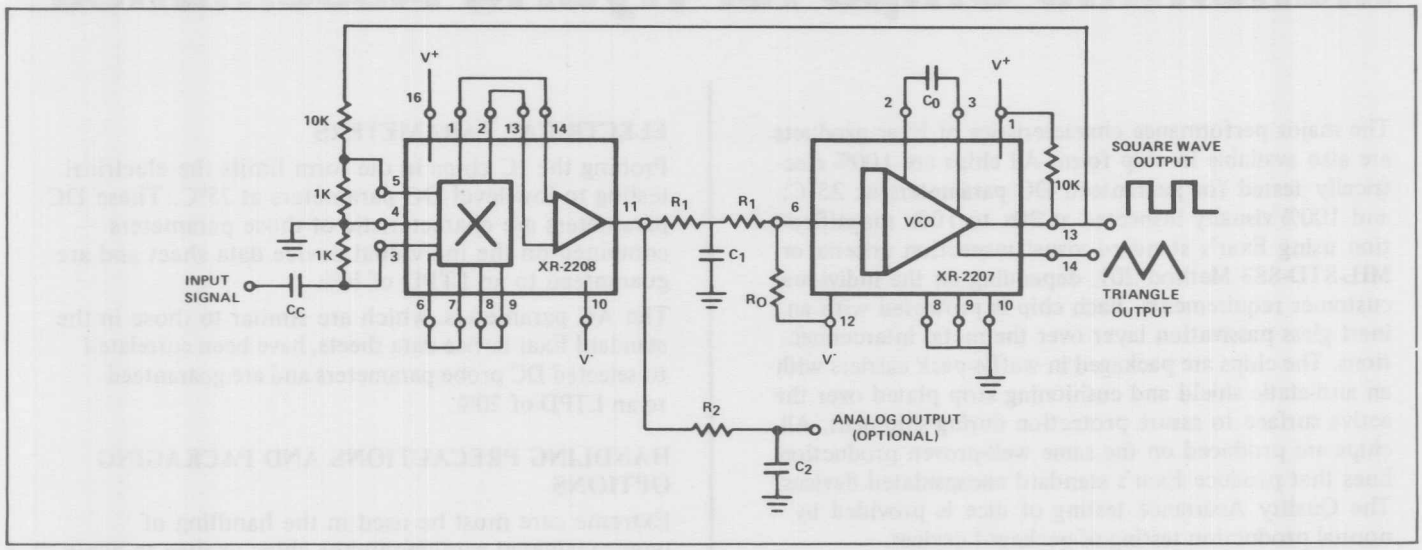


Figure 1. Circuit Interconnections for the Precision PLL System Using the XR-2207 and the XR-2208 Monolithic Circuits. (Split-supply Operation, ±6V to ±13V.)

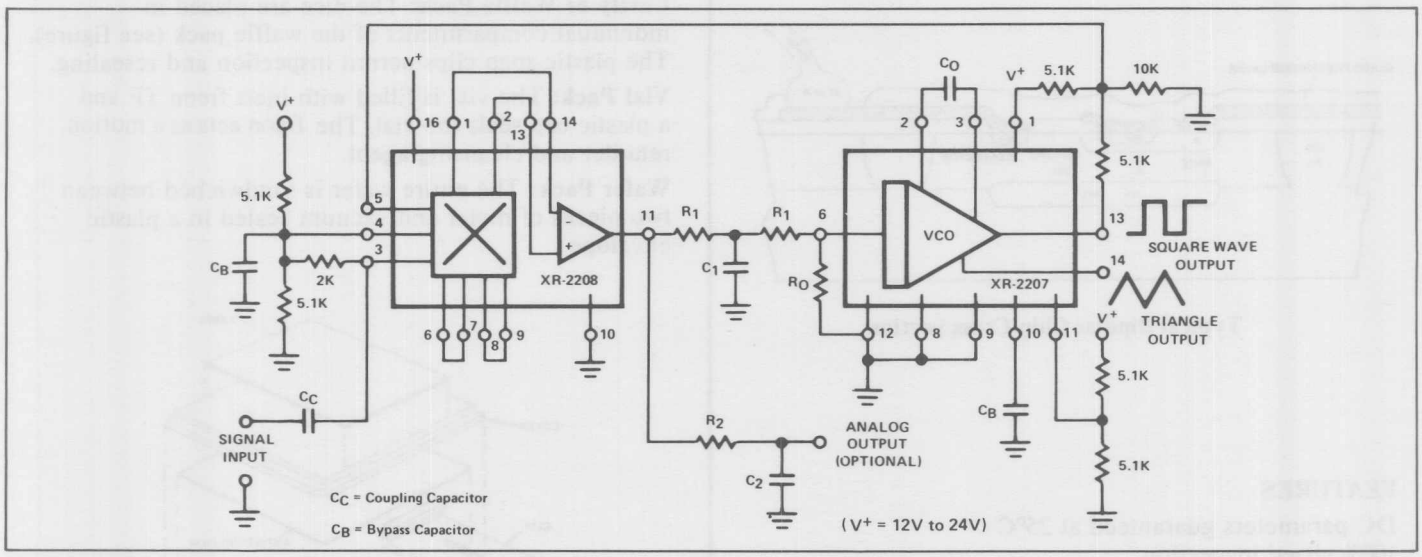


Figure 2. Circuit Interconnections for Single Supply Operation.

TABLE 1

Phase-Locked Loop Design Equations*

(1) Center Frequency: $f_0 = \frac{1}{R_0 C_0}$ Hz

(2) Lock Range: $(\Delta f_L / f_0) = (0.9)(R_0/R_1)$

(3) Phase Detector Gain: $K_\phi = 0.5\ V_{cc}$ volts/radian
Where $V_{cc} = V^+$ for split supply; $V_{cc} = V^+/2$ for single supply.

(4) VCO Conversion Gain: $K_v = \frac{1}{2\ V_{cc} C_0 R_1}$ rad/sec/volt

(5) Loop Gain: $K_L = K_\phi K_v = \frac{0.25}{C_0 R_1}$ sec^{-1}

(6) Low Pass Filter Time Constant: $\tau = \frac{C_1 R_1}{2}$ sec.

(7) Loop Damping: $= \frac{1}{2\sqrt{\tau K_L}} = \sqrt{\frac{2\ C_0}{C_1}}$

(8) Capture Range:

a) Underdamped Loop ($\xi < 1/2$):

$$(\Delta f_c / f_0) = \frac{0.8^{R_0}}{R_1} \sqrt{\frac{C_0}{C_1}}$$

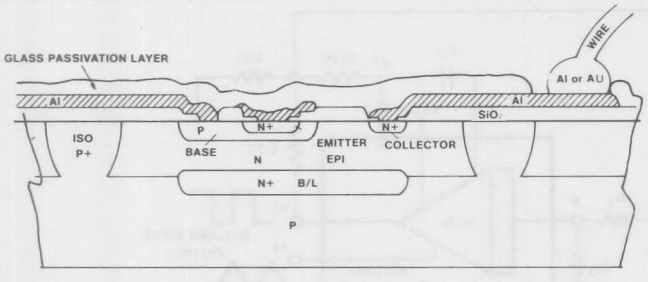
b) Overdamped Loop ($\xi > 1$):

$$(\Delta f_c / f_0) = 0.8(R_0/R_1)$$

*See Figures 1 and 2 for component designation.

Monolithic Chips for Hybrid Assemblies

The major performance characteristics of Exar products are also available in chip form. All chips are 100% electrically tested for guaranteed DC parameters at 25°C; and 100% visually inspected at 30x to 100x magnification using Exar's standard visual inspection criteria or MIL-STD-883 Method 201, depending on the individual customer requirements. Each chip is protected with an inert glass passivation layer over the metal interconnections. The chips are packaged in waffle-pack carriers with an anti-static shield and cushioning strip plated over the active surface to assure protection during shipment. All chips are produced on the same well-proven production lines that produce Exar's standard encapsulated devices. The Quality Assurance testing of dice is provided by normal production testing of packaged devices.



Typical Bipolar Chip Cross Section

FEATURES

DC parameters guaranteed at 25°C
100% visual inspection
Care in packaging
100% Stabilization Bake (Wafer Form)
10% LTPD on DC Electrical parameters

CHIPS IN WAFER FORM

Probed and inked wafers are also available from Exar. The hybrid microcircuit designer can specify either scribed or unscribed wafers and receive a fully tested silicon wafer. Rejected die are clearly marked with an ink dot for easy identification in wafer form.

ELECTRICAL PARAMETERS

Probing the IC chips in die form limits the electrical testing to low level DC parameters at 25°C. These DC parameters are characteristic of those parameters contained on the individual device data sheet and are guaranteed to an LTPD of 10%.

The AC parameters, which are similar to those in the standard Exar device data sheets, have been correlated to selected DC probe parameters and are guaranteed to an LTPD of 20%.

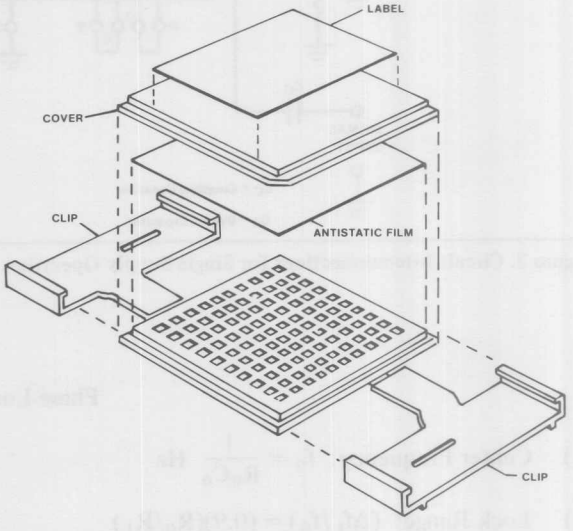
HANDLING PRECAUTIONS AND PACKAGING OPTIONS

Extreme care must be used in the handling of unencapsulated semiconductor chips or dice to avoid damage to the chip surface. Exar offers the following three handling or packaging options for monolithic chips supplied to the customer:

Cavity or Waffle Pack: The dice are placed in individual compartments of the waffle pack (see figure). The plastic snap clips permit inspection and resealing.

Vial Pack: The vial is filled with inert freon TF and a plastic cap seals the vial. The freon acts as a motion retarder and cleansing agent.

Wafer Pack: The entire wafer is sandwiched between two pieces of mylar and vacuum sealed in a plastic envelope.



Typical Cavity Pack (Waffle Pack)